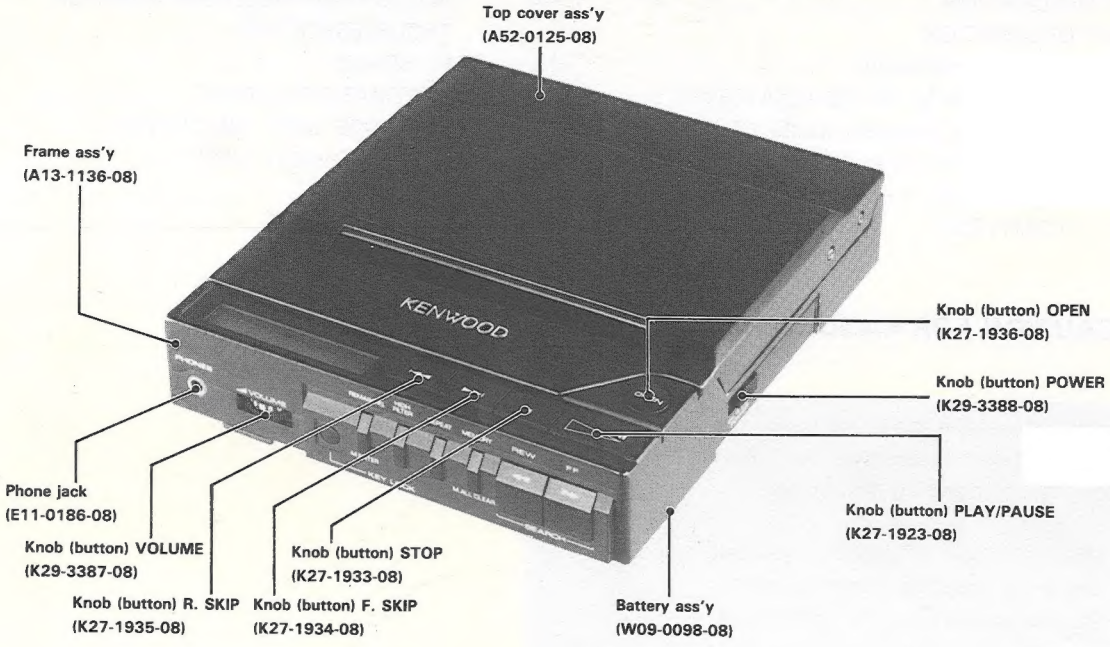
COMPACT DISC PLAYER

DPC-77

SERVICE MANUAL

KENWOOD

B51-3483-00(T)667



SPECIFICATIONS

PICK UP

Type ..... Optical pick up
Laser type ..... Semiconductor laser

AUDIO

Channels ..... 2 channels
Frequency response ..... 20 Hz - 20,000 Hz, ±1 dB
Dynamic Range ..... 90 dB (at 1 kHz)
Total harmonic distortion ..... 0.01% (at 1 kHz)
Channel separation ..... 75 dB (at 1 kHz)
Wow & flutter ..... Below measurable limit
Output terminals ..... PHONES jack (3.5 mm stereo mini jack)
LINE OUT jack (3.5 mm stereo mini jack)
DIGITAL OUT jack (3.5 mm mono mini jack)
Input terminals ..... DC IN (external power supply jack 5.5 mm)
Output level ..... 20 mW + 20 mW (16-ohm, at 1 kHz)
Line output ..... 1 V (10 k-ohm at 1 kHz)

GENERAL

Power requirements ..... 6 V DC built-in rechargeable lead acid battery,
120 V AC 60 Hz (U.S.A. and Canada type, using the provided AC adaptor) or
110-120/220-240 V AC, 50/60 Hz (All other type, using the provided AC adaptor)
Power consumption ..... 1.8 W
Battery life ..... About 5.5 hours (continuous repeat playback)
Charging time ..... Approximately 8 hours
Dimensions ..... 128 × 34.9 × 145 mm (main body)
Weight ..... 750 g
Accessories ..... Connection cord ×1
AC adaptor ×1
Carrying belt ×1
Car audio cassette adaptor (CAC-1) ×1

KENWOOD follows a policy of continuous advancements in development. For this reason specification may be changed without notice.

DANGER
INVISIBLE LASER RADIATION WHEN OPEN AND INTERLOCK DEFEATED. AVOID DIRECT EXPOSURE TO BEAM.

*** Refer to parts list on page 79.**

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CONTENTS

PRECAUTION FOR HANDLING LASER PICKUP

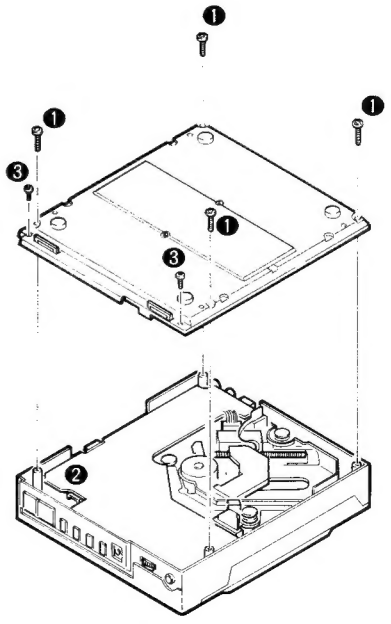
The pickup used in this unit is easily damaged by static electricity. Take careful note of the following points when soldering and handling this divice.

1. Make sure to first discharge yourself to ground.
2. Use a grounded-tip soldering iron.
3. Ground the divice while soldering-in.
4. Cover the work table with conductive, grounded panel to insure an adequate static discharge path.

Don't open the divice of repairing parts from the anti-static bag, if not necessary.

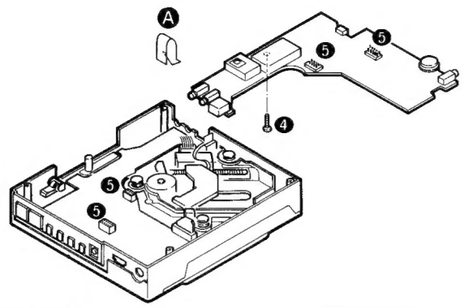
DISASSEMBLY FOR REPAIR

1. Remove the 4 screws (❶) fixing the cover (bottom case) to the chassis, and then take off the cover (bottom case).
2. At this time, disconnect the connector linking the battery on the cover (bottom cover) to the PC board (❷).
3. Remove the 2 screws (❸) fixing the holder to the cover (bottom case), and remove the holder.

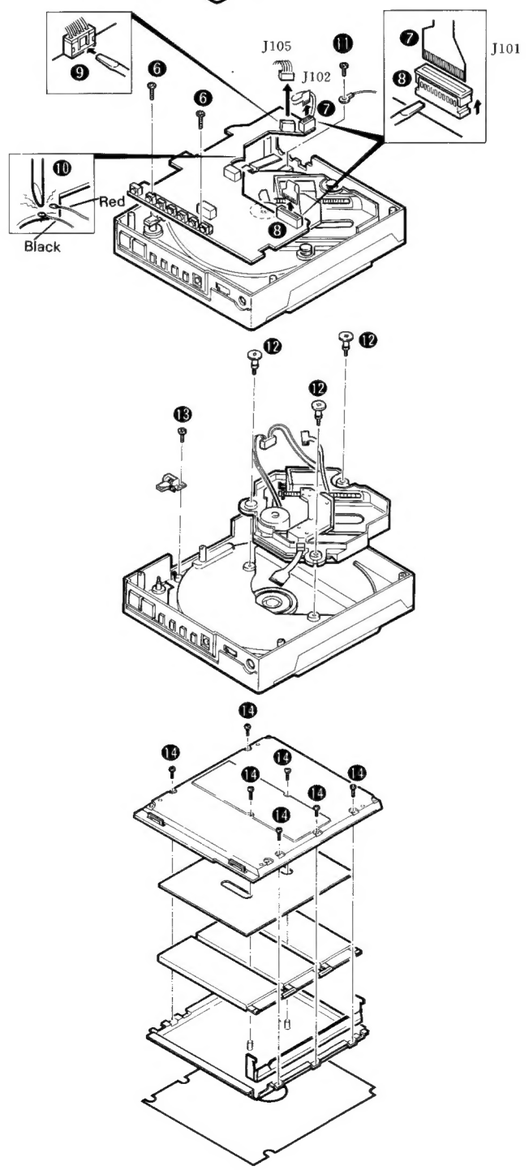


DISASSEMBLY FOR REPAIR

4. Remove the screw (❹) fixing the PC board to the chassis.
5. Disconnect the connector linking the PC boards (❺).
6. Take out the PC board in the direction of the arrow (Ⓐ).



7. Remove the 2 screws (❻) fixing the PC board to the chassis.
8. Remove the flexible PC boards attached to pin connectors J101 and J102 (❼, ❽).
9. Using a flat-blade screwdriver, disconnect the connector attached to pin connector J105 (❾).
10. Using a soldering iron, remove the cord attached to the PC board and motor on the Mechanism Ass'y (❿).
11. Remove the screw (⓫) fixing the cord from the PC board to the chassis.
12. Remove the 3 screws (⓬) fixing the Mechanism Ass'y to the chassis, and then take out the Mechanism Ass'y.
13. Remove the screw (⓭) fixing the spring for the OPEN button to the chassis, and then take out the spring.



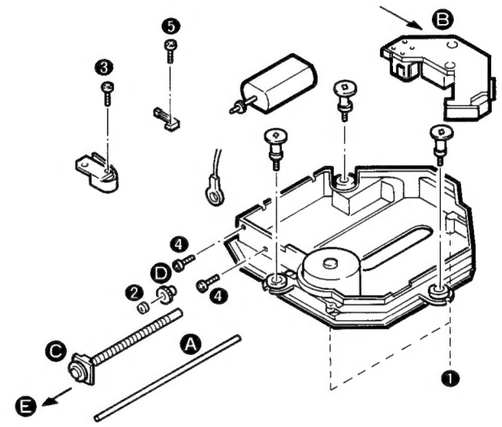
Removing the battery

Remove the 7 screws (⓮) fixing the cover (bottom case) and battery, and then take out the battery.

DISASSEMBLY FOR REPAIR

Disassembly of Mechanism

1. Loosen the 2 screws (❶) holding down the PU shaft, and then pull out the PU shaft (Ⓐ).
2. Take out the PU shaft in the direction of the arrow (Ⓑ), separating it from feed screw Ⓒ.
3. Remove the E ring (❷) holding gear Ⓓ, and then take out gear Ⓓ.
4. Remove the screw (❸) on the metal hardware holding feed screw Ⓒ, and then take out the metal hardware.
5. Disengage the claw of the locking hardware holding feed screw Ⓒ to the Mechanism Ass'y, and then pull out feed screw Ⓒ in the direction of the arrow (Ⓔ).
6. Remove the 2 screws (❹) fixing the motor, and then take out the motor. (The motor is attached to the Mechanism Ass'y and by double-side adhesive tape.)
7. Remove the screw (❺) fixing the leaf switch to the Mechanism Ass'y, and then take out the leaf switch.



1. Feed motor current check

Apply a 1.5 V DC supply to the feed motor, and the check the current value.

The current should be about 70 mA through the pickup movement from the innermost to the outermost position.

2. Lead-in time check

Measure the lead-in time using a test disc from SONY (YEDS-18, Type 4), and adjust it to between 4 min. 30 sec. and 5 min. The lead-in time can be changed by adjusting the leaf switch position.

3. Leaf switch replacement

Similar to the head replacement procedure, remove the feed screw and head before replacing the leaf switch. During this operation, take care so as not to damage the screws.

Check the lead-in time after replacement.

4. Joint arm replacement

In addition to the head replacement operations, remove the joint arm from the laser pickup and proceed with the job. Take care so that bonding, etc., does not get on the laser pickup.

5. Disc table replacement (motor or mechanism chassis)

The disc table is attached to the disc motor shaft by adhesion, so these parts should be replaced as a set.

These parts are also supplied in the form of an assembly. For replacement, change all of the parts as a whole.

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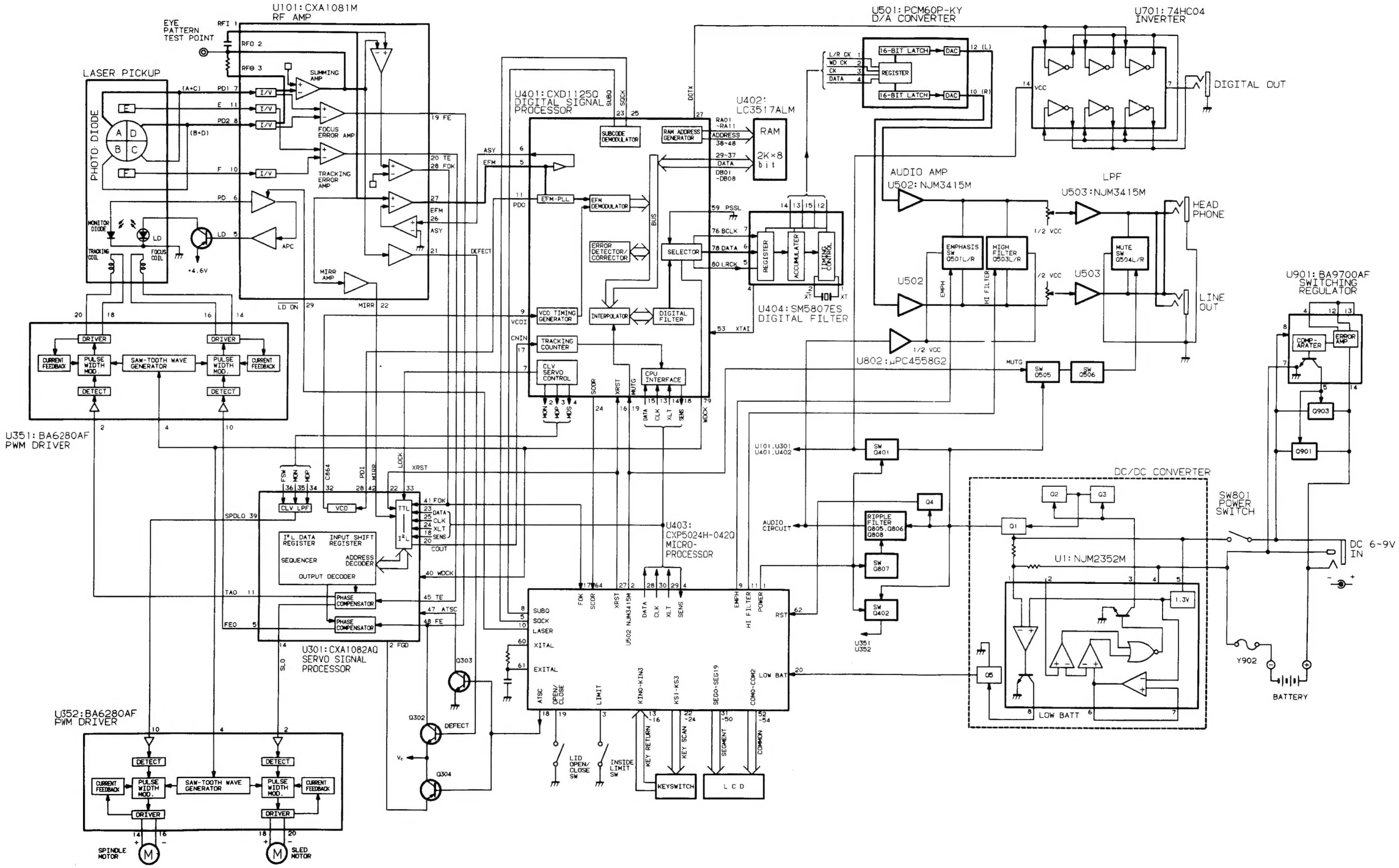
BLOCK DIAGRAM



Unpacking

Unpack the unit carefully and make sure that all accessories and cables are put aside so they will not be lost.
Examine the unit for any possibility of shipping damage. If your unit is damaged or fails to operate, notify your dealer immediately. If your unit was shipped to you directly, notify the shipping company without delay. Only the consignee (the person or company receiving the unit) can file a claim against the carrier for shipping damage.
We recommend that you retain the original carton and packing materials for use should you transport or ship the unit in the future.

Before applying power of AC adaptor

Important!

USA and Canada
Unit shipped to the above are not equipped with an AC voltage selector switch and the discussion of such a switch that follows should be disregarded.

All other countries
AC adaptor shipped to countries other than the above are equipped with an AC voltage selector switch on the top cover. Refer to the following paragraph for the proper setting of this switch.

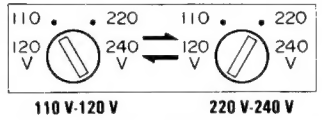
AC voltage selection

AC adaptor operates on 110 ~ 120 volts or 220 ~ 240 volts AC. Before connecting the power cord to your AC outlet, make sure that the setting position of this switch matches your line voltage. If not, it must be set to your voltage in accordance with the following direction.

Note:
Our warranty does not cover damage caused by excessive line voltage due to improper setting of the AC voltage selector switch.

WARNING:

TO PREVENT FIRE OR ELECTRIC SHOCK, DO NOT EXPOSE THIS APPLIANCE TO RAIN OR MOISTURE.



Move switch lever to match your line voltage with a small screwdriver or other pointed tool.

AC voltage selector switch

Fig. 1

Before plugging in this unit, make sure that the position of the AC Voltage Selector conforms to your line (mains) voltage. If not, it must be reset. See Fig. 1.

WARNING NOTICE:

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Before operating the unit (precautions)

■ Avoid placing the unit in the following places.

- Under direct sunlight or near a source of heat such as a heater. Especially, never leave the unit in a closed automobile, or on the dashboard or parcel shelf.
- Near a source of strong magnetism, such as a magnet or speaker.
- On an unstable shelf or in a place subject to frequent vibrations.
- Where there is excessive dirt or moisture.

■ Also observe the following to avoid a malfunction or damage to the unit.

- Do not remove the case or attempt to disassemble the unit.
- Do not touch the disc surface or lens.
- Do not drop or apply strong shock to the unit.

■ In case of abnormal smell

- If an abnormal smell or smoke is detected, immediately turn the power OFF and pull out the power cord. Contact your dealer or nearest service station.

■ Note on condensation

- When the room or car compartment heater is first turned on, or when there is much vapor or moisture in the air, dew may condense on the internal lens of the unit, causing a malfunction. In this case, set the POWER switch to OFF, leave the unit for at least an hour, then insert a disc and try again.

■ Notes on headphones

- As a CD contains very little noise, the listener tends to increase the volume level too high. To protect your ears from too strong of a stimulation, be careful to adjust the headphone volume to an optimum level.
- For safety in traffic, do not use headphones while driving an automobile, riding a bicycle, etc.
- Be careful not to fall asleep while listening to music through headphones.

Fig. 2

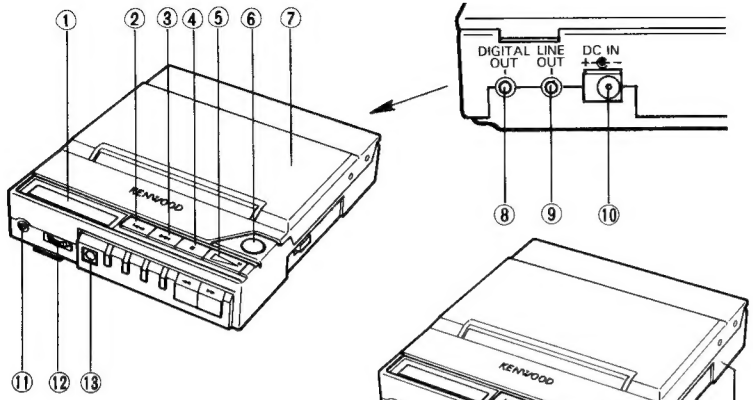
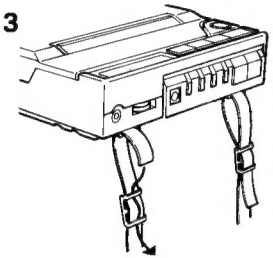
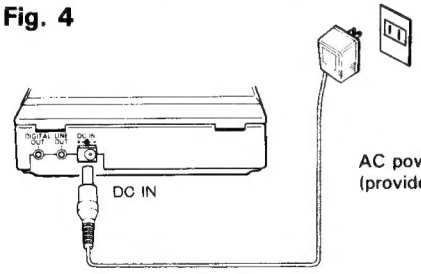


Fig. 3



Carrying belt (provided)

Fig. 4



To AC outlet

AC power adaptor
(provided)

Fig. 5

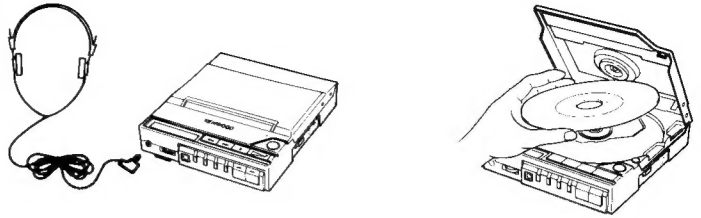


Fig. 6

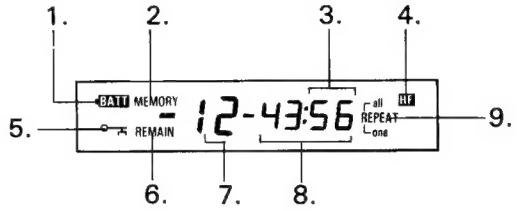


Fig. 7

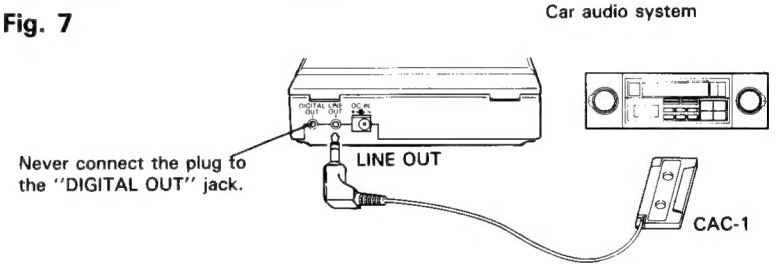
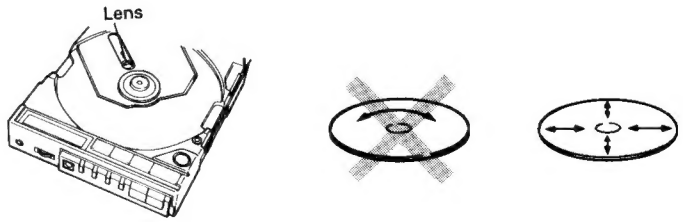


Fig. 8



Controls, connectors and indicators <Fig. 2>

① **Display**
The LCD shows all necessary information, including the playing time and track number.

② ③ **F-SKIP [►►I] and R-SKIP [I◄◄] buttons**
When one of these buttons is pressed the playback position skips to the beginning of the track (tune) before or after the current track being played.
To play a track after the current track, press the "►►I" button for the same number of times as the difference between the desired track and the current track.
When the "I◄◄" button is pressed once, the currrent track is played from the beginning: afterward, the playback position skips to the previous track every time the "I◄◄" button is pressed.

④ **STOP [■]/M.CLEAR button**
When this button is pressed during playback or when paused, it is completely stopped.
When pressing in stop mode, one of the programmed track number will be deleted, as this time the track number which was programmed as the next program number will be displayed.

⑤ **PLAY/PAUSE [▻] button**
When a disc has been inserted, press this button to start playback. Pressing the button during playback causes it to pause temporarily.

⑥ **OPEN button**
When this button is pressed, the lid is unlocked and opened a little.

⑦ **Lid**
To insert or take out a disc, open the lid by pressing the OPEN button.

⑧ **DIGITAL OUT jack**
Used to connect a digital amplifier or a home audio system with a digital input terminal.

⑨ **LINE OUT jack**
Used to connect a home audio system (with the provided connection cord), or a car audio system (with the provided Car Audio Cassette Adaptor).

⑩ **DC 6V-9V power supply jack**
Used to connect the provided AC adaptor. Although a commercially-available car power adaptor can also be connected here, be very careful of the ⊕/⊖ polarity of the connector, plug size, the power capacity, etc., for these do not always match the characteristics of this unit.

⑪ **PHONES jack**
Connect headphones here.

⑫ **VOLUME control**
Turn to adjust the sound volume.

⑬ **KEY LOCK button**
When this button is pressed once during playback, the " ⊶ " mark appears on the display ①, and button ② to ⑤ and ⑭ to ⑲ become inoperative, thus preventing operation mistakes. Pressing the button again releases the lock condition. If this button is pressed during playback when in a place subject to strong vibrations, such as in a car, sound skip due to vibrations will be reduced.

⑭ **REMAINING/M.ENTER button**
When this button is pressed during playback, the number of remaining tracks and their playing time appears on the display. This button is also used as the memory entry key when programming tracks. The remaining time is not displayed during memory playback.

⑮ **HIGH FILTER button**
Press this button to engage the high-frequency cut filter.

⑯ **REPEAT button**
When this button is pressed, the memory repeat, one-track repeat or all-track repeat function is activated.

⑰ **MEMORY/M.ALL CLEAR button**
Press this button when programming tracks into memory. This button is also used as the memory all clear key, to clear all of the programmed track numbers.

⑱ ⑲ **REVERSING [◄◄]/FAST-FORWARDING [►►] button**
During playback, pressing the FF "►►" button will fast-forward the playing position, and pressing the REW "◄◄" button will fast-reverse the playing position.

⑳ **POWER switch**
Set to ON to turn on the power of the unit.

㉑ **Built-in rechargeable battery**

How to attach the carrying belt

• *Attach the carrying belt as shown in the Fig. 3*

Notes on the power supply <Fig. 4>

■ Before operating the unit, be sure to charge the rechargeable battery.
■ To turn on the power of the unit, set the POWER switch to ON.
■ When the unit is not used, be sure to set the POWER switch to OFF (otherwise, the battery will be exhausted and its service life may be shortened).
■ After CD play, when about 30 seconds have elapsed in stop mode, the auto power-off function is activated, and the unit is automatically turned OFF to save power. To turn the power ON again, press the PLAY/PAUSE " ▷/II " button, or any other button.

■ How to charge the rechargeable battery

- Connect the provided AC adaptor as shown in the Fig. 4.
- The time required for a full charge is about 8 hours.
- When the unit is operated while charging the battery, a slightly longer charging time will be required.

Notes:

- When charging the battery, be sure to use the provided AC adaptor.
- To prevent leakage of the battery, do not place the battery standing up or on a slant while charging.
- Do not charge the battery in a place with poor ventilation, such as enclosed in a vinyl envelope.
- Be sure to charge the battery whenever it is exhausted.
- When the unit is not used for an extended period of time, charge it at least once every 6 months.
- If battery fluid leaks on the skin or clothes, immediately clean with running water.
- Do not place the unit into a fire.
- Be careful not to recharge the battery for 24 hours or more, as overcharging will shorten the battery life.

■ How to operate the unit using the provided AC adaptor

To operate the unit on a household power supply, connect the AC adaptor as shown in the Fig. 4.

Cautions:

- When the unit is not to be used, be sure to disconnect the AC adaptor from the power outlet.

To avoid electrical hazards

- When the unit is to be powered on a household AC power supply, be sure to use the provided AC adaptor. If a different type of AC adaptor is used, the unit could be damaged.
- When the AC adaptor is not to be used, be sure to disconnect it from the power outlet.
- When disconnecting the AC adaptor plug from the unit, be sure to grasp the plug, and do not pull on the cord.
- Do not touch the unit with wet hands.

Playback of a compact disc

Before starting playback, set the VOLUME control to the "0" position.
As a Compact Disc contains very little noise, a sudden loud sound could be output if the VOLUME control is adjusted too high: this could cause serious damage to your ears.

■ Preparation <Fig. 5>

- Connect the headphones to the PHONES jack.
- Press the OPEN button to open the lid.
- Insert the disc with the labeled side facing up.
- Close the lid securely, until a click sound is heard.
- Set the POWER switch to ON. The disc starts rotating automatically, and about 3 and 4 seconds later, the total number of tracks contained on the disc and their total playing time will be displayed in the display window.

■ Normal playback

1. Press the PLAY/PAUSE " ▷/II " button.
   The disc is played from track No. 1.
2. Adjust the volume with the VOLUME control.
3. To pause playback temporarily, press the PLAY/PAUSE " ▷/II " button again. (At this time, the time display will blink.)
4. To stop playback, press the STOP " ■ "/M. CLEAR button.

■ Skip play and fast-forwarding/reversing

1. Press the F-SKIP "▶▶I" button to quickly advance the playing position to the beginning of the next track. Pressing the F-SKIP "▶▶I" button repeatedly will advance the playing position to the beginning of the track ahead of the current track by the number of times that the button is pressed.
2. Press the R-SKIP "I◀◀" button to quickly return the playing position to the beginning of the current track. Pressing the R-SKIP "I◀◀" button repeatedly will return the playing position to the beginning of the track in back of the current track by the number of times that the button is pressed.

- Even in stop mode, the playing position can be moved to the beginning of the desired track by pressing the F-SKIP "▶▶I" or R-SKIP "I◀◀" button.

3. During playback, pressing the FF "▶▶" button will fast-forward the playing position, and pressing the REW "◀◀" button will fast-reverse the playing position.

■ Play repeatedly

- With the repeat function, whole tracks on the disc, only a desired track, or the programmed tracks can be played repeatedly.

1. When the REPEAT button is pressed once, the "REPEAT-one" appears in the display and the currently playing track will be played repeatedly.
2. When the REPEAT button is pressed once more, the "REPEAT-all" appears, and all of the tracks on the disc will be played repeatedly. During memory play, all of the programmed tracks will be played repeatedly.
3. When the REPEAT button is pressed again, the "REPEAT" goes off and the repeat function is disengaged.

- Repeat play can be activated even in stop mode.

■ Memory playback

Memory play allows the tracks to be played in any desired order.

■ How to program tracks

Programming tracks is possible only when the unit is in stop mode. First, press the STOP " ■ "/M.CLEAR button to stop play.

1. Press the MEMORY/M.ALL CLEAR button. The "MEMORY" indicator lights up and the program number ("1" at first) will be displayed.

2. Select the track to be programmed by pressing the "▶▶|" or "|◀◀" button. (The following example shows that the 3rd track is programmed.)

3. Press the REMAINING/M.ENTER button to program the track. The next program number will be displayed.

4. Repeat procedures 2. and 3. to program more tracks. Up to 16 tunes can be programmed for memory play.

- During programming, if you wait for an interval of more than about 30 seconds, the automatic power-off function is activated, and all programmed memories will be cleared. In this case, to program the tracks again, first press the MEMORY/M.ALL CLEAR button.

■ How to start memory playback

1. Press the PLAY/PAUSE " ▻ " button.

- During memory playback, skipping tracks, or fast-forwarding in the programmed order is possible using the F-SKIP "▶▶|", R-SKIP "|◀◀", FF "▶▶", or REW "◀◀" button.
- During memory playback, single track repeat, or all repeat, play is possible within the programmed tracks by pressing the REPEAT button.

2. To stop memory playback, press the STOP " ■ "/ M.CLEAR button.

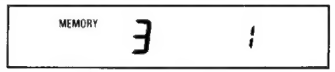
Note:

When the STOP " ■ "/M.CLEAR button is pressed in stop mode, any programmed tracks will be sequentially cleared, in the order in which they were programmed.

■ To check the program contents

Set the unit to stop mode.

1. Press the REMAINING/M.ENTER button.
   The first program number and the corresponding track number will be displayed.



2. In this way, the memory contents will be displayed sequentially by pressing the REMAINING/M.ENTER button.

- When the program number next to the last programmed number is displayed, pressing the button again will display the first programmed contents.

■ To change the program contents

Set the unit to stop mode.

1. Press the REMAINING/M.ENTER button repeatedly until the program number to be changed is displayed.
2. Select the desired track number by pressing the F-SKIP "▶▶|" or R-SKIP "|◀◀" button.
3. Press the REMAINING/M.ENTER button to place the selected track in memory.
4. To change another tracks, repeat procedure 1. to 3..

■ To delete part of the program

Set the unit to stop mode.

1. Press the REMAINING/M.ENTER button repeatedly until the track number to be deleted is displayed.
2. Press the STOP " ■ "/M.CLEAR button to delete the track number.

- At this time, the track number which was programmed as the next program number will be displayed.

■ To delete the entire program

Press the MEMORY/M.ALL CLEAR button and place the POWER switch to OFF, or open the lid. The entire programmed memory will be cleared.

■ 8 cm single CD can also be played.

This unit can play 8 cm single CDs directly without using an adaptor.

Caution:

- Do not use an adaptor sold for other models (otherwise the CD or this unit may be damaged.).

Display description <Fig. 6>

1. Lights when the rechargeable battery is exhausted. Charge it immediately.
2. Lights when programming or during memory play.
3. Displays the program number during programming.
4. Lights when the HIGH FILTER switch is engaged.
5. Lights when the KEY LOCK button is engaged.
6. Lights when the REMAINING button is engaged. At this time, "–" indicators are displayed in front of the track number and in front of the remaining time display.
7. Displays the total number of tracks on the disc, the number of remaining tracks, or the track number during play or programming.
8. Displays the total playing time of the disc, the elapsed time, or the remaining time.
9. Lights during repeat play.

CD playback in an automobile <Fig. 7>

- By using the provided Car Audio Cassette Adaptor (CAC-1), the CD playback sound can be played through your car stereo. (For details on this operation, please read the instruction manual provided with the CAC-1.)

Cautions:

- The CAC-1 cannot be used with some car audio cassette models.
- Do not leave the unit in a closed automobile where the temperature is expected to be high.
- Place the unit on a soft place where automobile vibrations are not easily transmitted.
- Pressing the "KEY LOCK" button reduces sound skip due to vibrations.

Playback through a home audio system

By using the provided home audio connection cord, the superb CD sound can also be enjoyed from the speakers of your home audio system.

- Power is supplied through the provided AC adaptor.
- Connect the provided connection cord to the LINE OUT jack of this unit, the white plug to the Left jack of the amplifier's CD or AUX input, and red plug to the Right jack. (Do not connect to the PHONO jacks.)
- When playing, set the VOLUME control to the "7" position for an optimum output level.

■ Playback using the "DIGITAL OUT" output

- The output from "DIGITAL OUT" can be connected to the digital input of other audio equipment, such as a digital amplifier, to obtain higher sound quality.
- When the "DIGITAL OUT" jack is not to be used, place the cap on it.

Cautions:

- Before making connections, be sure to turn the amplifier power off.
- If the CD player interferes with radio or TV reception. Place the CD player away from the radio or TV, or disconnect the power to the CD player.
- Never connect the output from the "DIGITAL OUT" jack to the analog input jack of an amplifier, as this will cause damage to the amplifier or speakers.

Simple care and maintenance

■ Cleaning the cabinet

When the cabinet gets dirty, wipe it with a dry cloth. If the stain is so serious that it cannot be removed with a dry cloth, moisten the cloth with a small amount of water. After wiping with the moistened cloth, do not forget to remove the moisture with a dry cloth.

■ Cleaning the lens

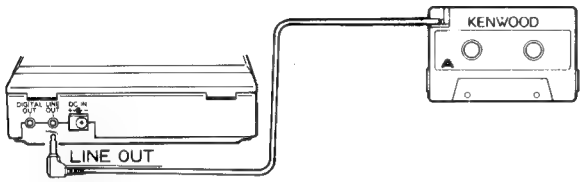
Clean the lens carefully, using a commercially-available camera lens blower, etc.

■ Care and maintenance of discs

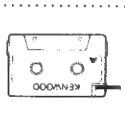
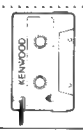
If dirt or dust is attached to the playing surface of a disc, clean it carefully using a commercially-available CD cleaning cloth, etc.
When wiping the disc, be sure to wipe it in a radial direction, as shown in the Fig. 8. (Do not use a record cleaner for ordinary disks.)
Avoid leaving discs under direct sunlight or in a place where the temperature is high.
When a disc is not to be used for a long period of time, do not leave it in the CD player.

Operations

1. Lower the volume of both the CD player and the car stereo to avoid sudden excessively large sound output.
2. **Connections:**
   Insert the plug of the cord extending from the CAC-1 into the CD player.



3. The **CAC-1** inserting direction differs for each type of car stereo used, and depends on the cassette insertion slot of the cassette deck section. Refer to the following chart for loading instructions.

	Auto-reverse cassette deck			Normal (one-direction)
Cassette insertion slot (Car stereo)				
CAC-1				
	Tape side to be played			
	For playback of upper side	For playback of lower side	For playback of upper side	Load with side A facing up
Notes		In this case, first replace the attached hooking prevention lug with the one provided.		
	If sound is not heard, or is very low, reverse the tape running direction to the opposite side.			

4. After placing the CAC-1 into the car stereo cassette insertion slot, raise the volume level of the car stereo to the normal listening position. Then adjust the volume of the CD player. (After this, use the car stereo control to adjust the volume level.)
5. To remove the CAC-1 from the car stereo, press the EJECT button in the same way as for cassette tapes.

Unusable Car Stereo Types

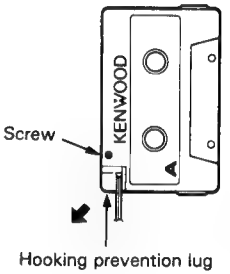
The CAC-1 cannot be used with the following types of car stereos.

a) One-direction cassette receivers in which the head is located on the left side.
b) Cassette receivers which function by detecting the tape tension. (In this case, when loading the CAC-1, it will be ejected.)
c) Car stereo models where the CAC-1 signal cord interfere with the insertion and removal of the CAC-1.

Replacement of Hooking Prevention Lug

To replace the attached hooking prevention lug, connected to the signal cord outlet of the CAC-1, with the one supplied, perform the following.

a) Loosen the screw located close to the cord outlet.
b) Remove the lug by pulling it in the direction of the arrow, as shown in the figure.
c) Insert the supplied lug by pushing it in the direction opposite to the arrow. (At this time, the lug is on side A.)
d) Tighten the screw.



The **CAC-1** is a Car Audio Cassette Adaptor which permits a portable CD player to be used in a car in combination with cassette car stereo equipment.

The **CAC-1** employs an electromagneticly coupled head, which does not directly contact the car stereo head, for higher fidelity sound.

Specifications

Frequency response	50 - 20,000 Hz (depending on the car stereo used)
Dimensions	102.4 × 12.1 × 63.8 mm
Weight	45 g
Cord length	1.5 m
Accessories	Hooking prevention lug × 1

CIRCUIT DESCRIPTION

DESCRIPTION OF COMPONENTS

Component	Use/Function	Operation/Condition/Compatibility
U1	Switching regulator	DC/DC converter switch.
U101	RF amplifier	See the IC description. (p.13)
U301	Servo amplifier	See the IC description. (p.19)
U302	Operation amplifier	Amplifies the feed motor drive signal.
U351	Actuator control	See the IC description. (p.24)
U352	Motor control	See the IC description. (p.24)
U401	Digital signal processor	See the IC description. (p.25)
U402	Static RAM	See the IC description. (p.51)
U403	Microprocessor	See the IC description. (p.48)
U404	Digital filter	See the IC description. (p.47)
U501	D/A converter	See the IC description. (p.52)
U502	Audio amplifier	Buffer amplifier for DAC output.
U503	LPF	Low-pass filter.
U701	6-INVERT	Digital out signal buffer
U802	Operational amplifier	1/2 Vcc generator for the audio circuit.
U901	Switching regulator	Controls the charging circuit.
Q1	DC/DC converter output switch	Turns the DC converter output ON/OFF.
Q2	DC/DC converter output switch control	Turns Q1 ON/OFF.
Q4	Reset switch	Turns the reset circuit ON/OFF.
Q5	Low battery indicator switch	Goes ON when the battery voltage is 5.5 V or less.
Q101	LD switch	Switches the pickup's laser diode ON/OFF.
Q302	Focusing signal switch	Holds the focusing offset position during playback of a scratched disc (DEFECT-H).
Q303	Tracking	Turns the ATSC circuit ON during KEY LOCK.
Q304	Focusing gain switch	Increases the focusing gain during KEY LOCK.
Q401	Power switch	Switches the power to the whole system, except for the CPU.
Q402	Actuator/motor driver power switch	Supplies power to the actuator and motor drive IC.
Q501	Emphasis	Applies emphasis when an emphasis signal is detected by the CPU.
Q503	High filter	When the key is pressed, the CPU outputs an ON/OFF signal to switch the filter circuit ON/OFF.
Q504	Muting	Mutes the audio signal.
Q505	Muting driver	Controls Q506. When the microprocessor outputs the muting signal, Q505 receives it and turns the signal level ON/OFF.
Q506	Muting driver	Turns the muting driver ON/OFF. If the supply voltage drops (to 3.5 V), Q507 goes OFF to turn the muting drivers ON.
Q805, 806, 808	Ripple filter	Ripple filter for the audio circuit power supply.
Q807	Ripple filter switch	Switches the audio circuit power ON/OFF according to an ON/OFF signal from the CPU.
Q901	Charger circuit switch	Turns the charger circuit ON/OFF.
Q903	Power switch	Turns the charging output voltage ON/OFF.

CIRCUIT DESCRIPTION

U101: RF AMPLIFIER FOR THE CD (CXA1081M)

Note: The following only describes the required features, as extracted from the Handbook.

General

The CXA1081M is an IC developed for use in Compact Disc players. It incorporates a 3-spot optical pickup RF output amplifier, a focusing error amplifier, a tracking error amplifier, and other signal processing circuitry, such as focus OK, mirror, defect, and EFM comparator circuits, as well as a laser diode APC (Automatic Power Control) circuit.

Features

- Operates on a signal +5 V power supply, as well as on a ±5 V dual-voltage power supply.
- Low power consumption (100 mW with ±5 V, 50 mW with +5 V).
- An APC circuit which accepts either a P-sub or N-sub laser diode.
- A minimum of external parts required.
- A disc defect detector circuit for improved playability.

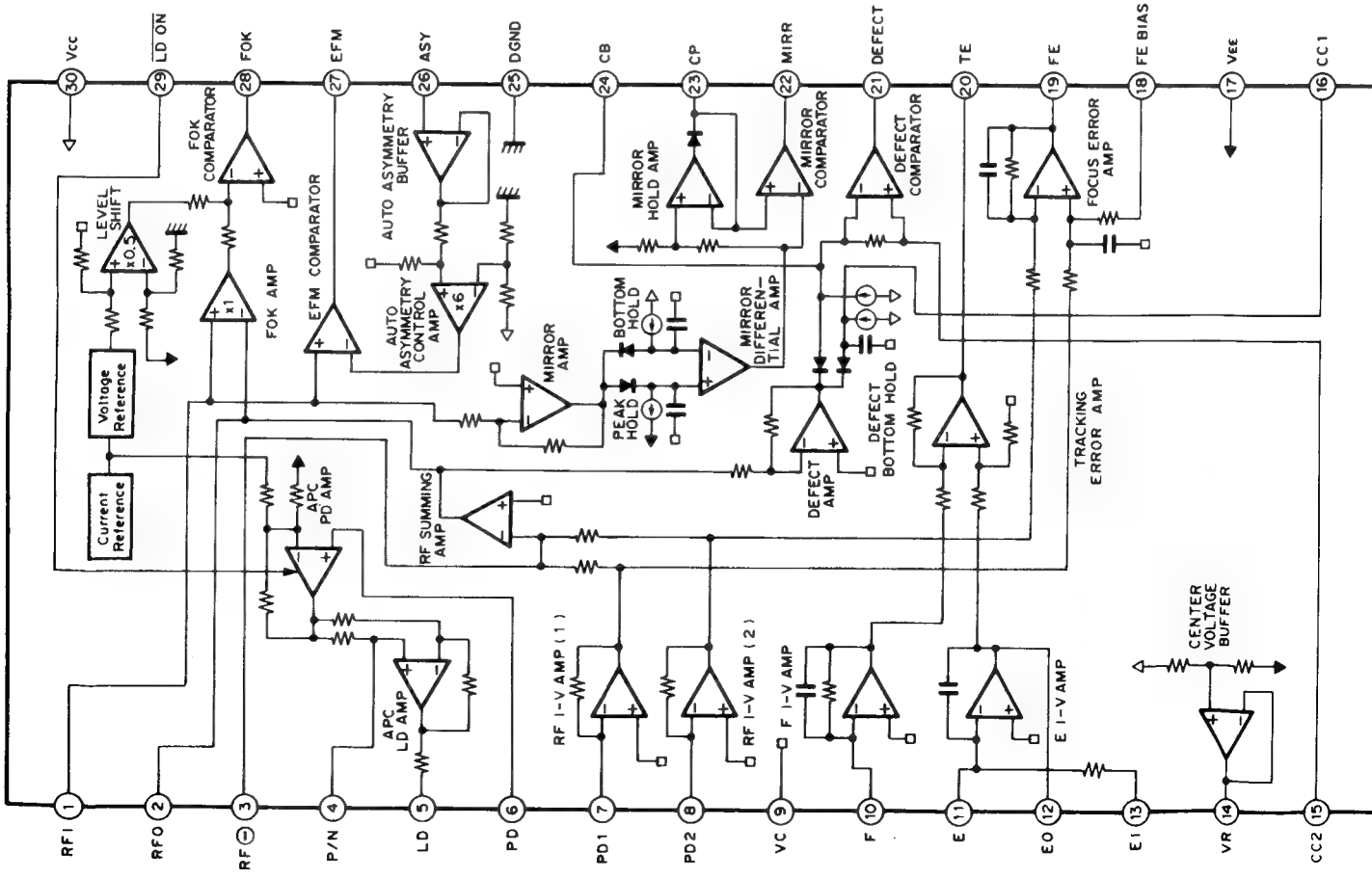
Structure

Bipolar silicon monolithic IC

Functions

- RF amplifier
- Focus OK detector circuit
- Mirror detector circuit
- Tracking error amplifier
- Defect detector circuit
- APC circuit
- EFM comparator
- Auto asymmetry control amplifier

Block diagram



CIRCUIT DESCRIPTION

Terminal explanation (V_{CC} = 2.5 V, V_{EE} = D_{GND} = −2.5 V, VC = GND)

Terminal No.	Terminal name	I/O	DC voltage (V)	Function
1	RFI	I	0	Input pin for the C-coupled signal output from the RF summing amplifier.
2	RFO	O	V_{RFO}	RF summing amplifier output pin. Used as the check point for the eye pattern.
3	RF⊖	I	0	RF summing amplifier feedback input pin.
4	P/N	I	0 (VC)	P-sub/N-sub select pin for the LD (Laser Diode). (DC voltage: in N-sub mode)
5	LD	O	−1.8	*APC LD amplifier output pin. (DC voltage: PD open in N-sub mode)
6	PD	I	0	*APC LD amplifier input pin. (DC voltage: open)
7	PD1	I	0	RF I-V amplifier (1) inverted input pin. Current input by connecting to the photodiode A + C terminal.
8	PD2	I	0	RF I-V amplifier (2) inverted input pin. Current input by connecting to the photodiode B + D terminal.
9	VC	—	0	Connected to GND when using a positive (+)/negative (−) dual-voltage power supply. Connected to VR (pin 14) when using a single-voltage power supply.
10	F	I	0	F I-V amplifier inverted input pin. Current input by connecting to the photodiode F terminal.
11	E	I	0	E I-V amplifier inverted input pin. Current input by connecting to the photodiode E terminal.
12	EO	O	0	E I-V amplifier output pin.
13	EI	I	0	E I-V amplifier feedback input pin. For E I-V amplifier gain adjustment.
14	VR	O	V_{CVO}	DC voltage output pin of (V_{CC} + V_{EE})/2.
15	CC2	I	1.0	Input pin for the C-coupled signal output from the defect bottom hold.
16	CC1	O	1.2	Defect bottom hold output pin.
17	V_{EE}	—	−2.5	Connected to the negative power supply when using a positive (+)/negative (−) dual-voltage power supply. Connected to GND when using a single-voltage power supply.
18	FE BIAS	I	0	Bias pin on the focus error amplifier non-inverted side. For CMR adjustment of the focus error amplifier.
19	FE	O	V_{FEO}	Focus error amplifier output pin.
20	TE	O	V_{TEO}	Tracking error amplifier output pin.
21	DEFECT	O	V_{DFCTL}	Defect comparator output pin. (DC voltage: connected to a 10 k-ohm load).
22	MIRR	O	V_{MIRL}	Mirror comparator output pin. (DC voltage: connected to a 10 k-ohm load).
23	CP	I	−1.3	Mirror hold capacitor output pin. Mirror comparator non-inverted input.
24	CB	I	0	Defect bottom hold capacitor connect pin.
25	DGND	—	−2.5	Connected to GND when using a positive (+)/negative (−) dual-voltage power supply. Connected to GND (V_{EE}) when using a single-voltage power supply.
26	ASY	I	—	Auto asymmetry control input pin.
27	EFM	O	V_{EFMH}	EFM comparator output pin. (DC voltage: connected to a 10 k-ohm load).
28	FOK	O	V_{FOKL}	FOK comparator output pin. (DC voltage: connected to a 10 k-ohm load).
29	LD ON	I	−2.5 (DGND)	LD ON/OFF select pin. (DC voltage: when LD ON)
30	V_{CC}	—	2.5	Positive power supply.

*APC: Automatic Power Control

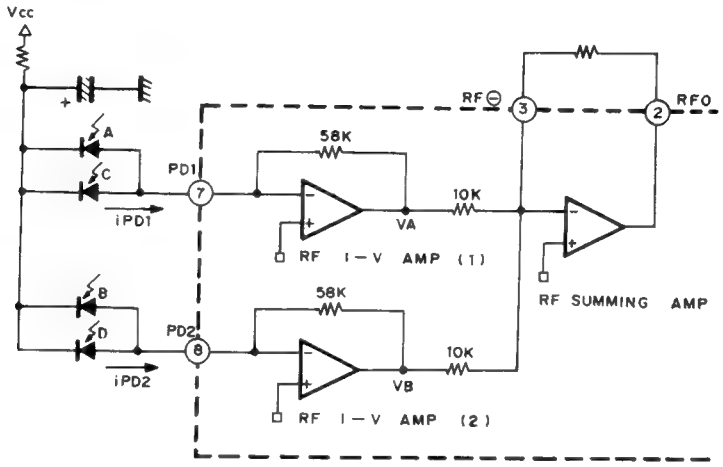
CIRCUIT DESCRIPTION

FUNCTION EXPLANATION

RF amplifier

The photodiode current input to the input pins (PD1, PD2) is converted to a voltage by an equivalent resistance of 58 k-ohms in RF I-V amplifier (1) and (2) respectively.

The voltage which is converted from the current of the photodiode (A+B+C+D) is added in the RF summing amplifier and is output from the RFO pin. The eye pattern can be checked at this pin.



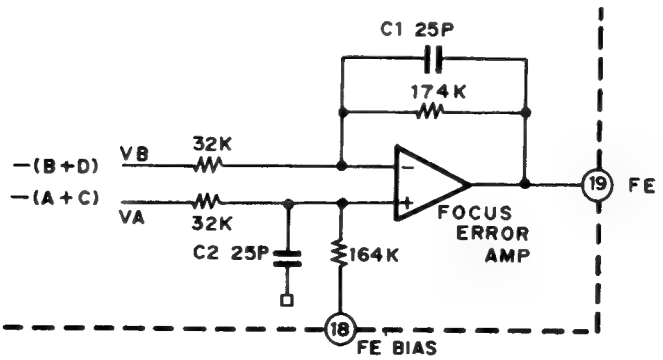
RF I-V AMPLIFIER

The low frequency component of the RFO output voltage, V_{RFO}, is represented by the following equation:

$$V_{RFO} = 2.2 \times (V_A + V_B)$$
$$= 127.6 \text{ k-ohms} \times (i_{PD1} + i_{PD2})$$

Focus error amplifier

The difference between the RF I-V amplifier (1) output (VA) and the RF I-V amplifier (2) output (VB) is calculated, and the current of the photodiode (A+C−B−D) is converted to a voltage and output.



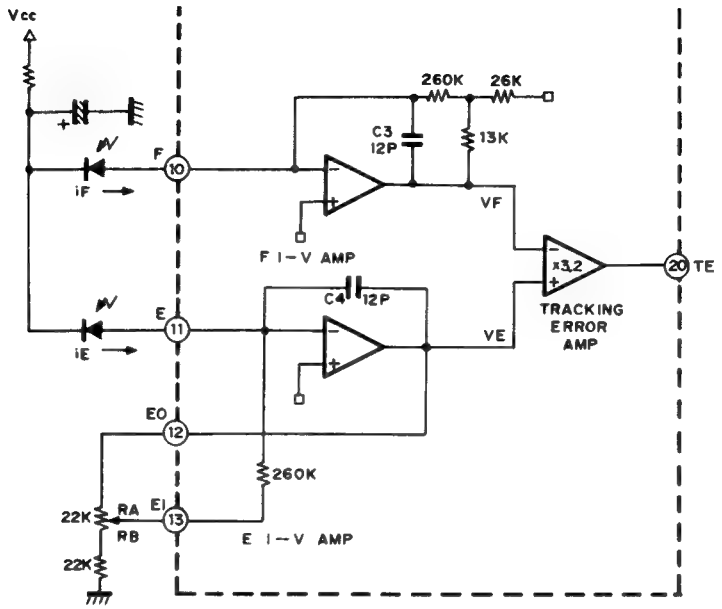
The FE output voltage (low frequency) is represented by the following equation:

$$V_{FE} = 5.4 \times (V_A - V_B)$$
$$= (i_{PD2} - i_{PD1}) \times 315.4 \text{ k-ohms}$$

The common mode rejection ratio of the VR connected to pin ⑱ is maximized when the composite impedance to GND is around 10 k-ohms (with a VR resistance of around 40 k-ohms).

CIRCUIT DESCRIPTION

Tracking error amplifier



The current from the side spot photodiodes is input to pins E and F and is converted to a voltage by the E I-V amplifier and F I-V amplifier respectively.
That is:

$V_F = iF \times 403$ k-ohms

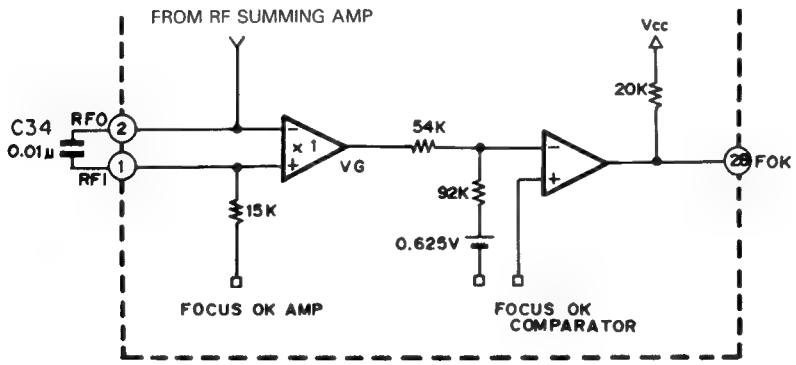
$V_E = iE \times 260$ k-ohms $\times R_A/(R_B + 22\ k) + (R_A + 260\ k)$

The difference between the E I-V amplifier and the F I-V amplifier is calculated by the tracking error amplifier, and the photodiode (E-F) current is converted to a voltage and output.

$V_{TE} = (V_E - V_F) \times 3.2$

$= (iE - iF) \times 1290$ k-ohms

Focus OK circuit



The focus OK circuit creates a timing window, turning the focusing servo ON with the focus search status.
While an RF signal is present at pin ②, an HPF output is present at pin ①. At the same time, the LPF output (opposite phase) of the focus OK amplifier is obtained.
The focus OK output is inverted when $V_{RFI} - V_{RFO}$ is almost equal to -0.37 V.

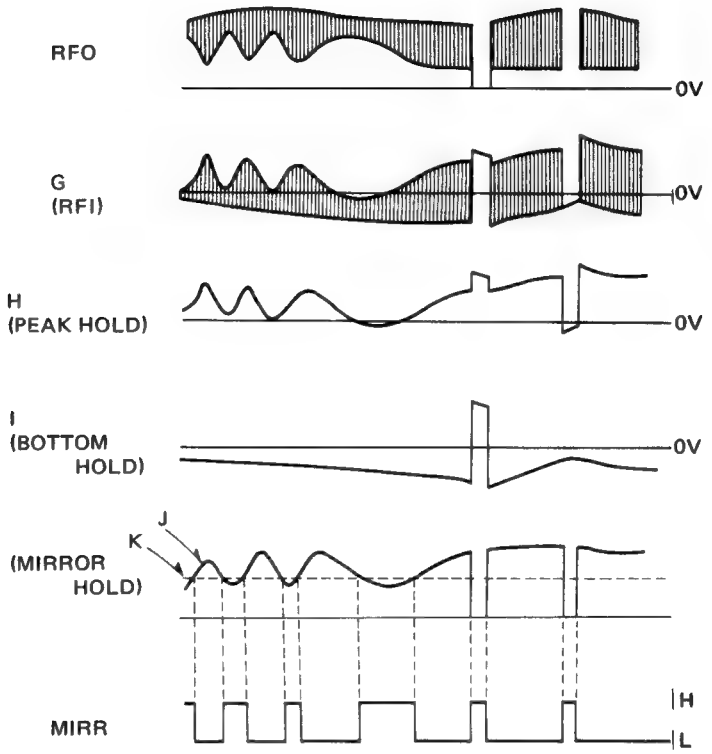
C34 is used to determine the time constants of the EFM comparator, the HPF in the mirror circuit, and the LPF in the focus OK amplifier. Normally, C34 = 0.01 μF is selected, with fc = 1 kHz. This will prevent degradation of the block error rate due to an RF envelope lack caused by cracks, etc. on the disc.

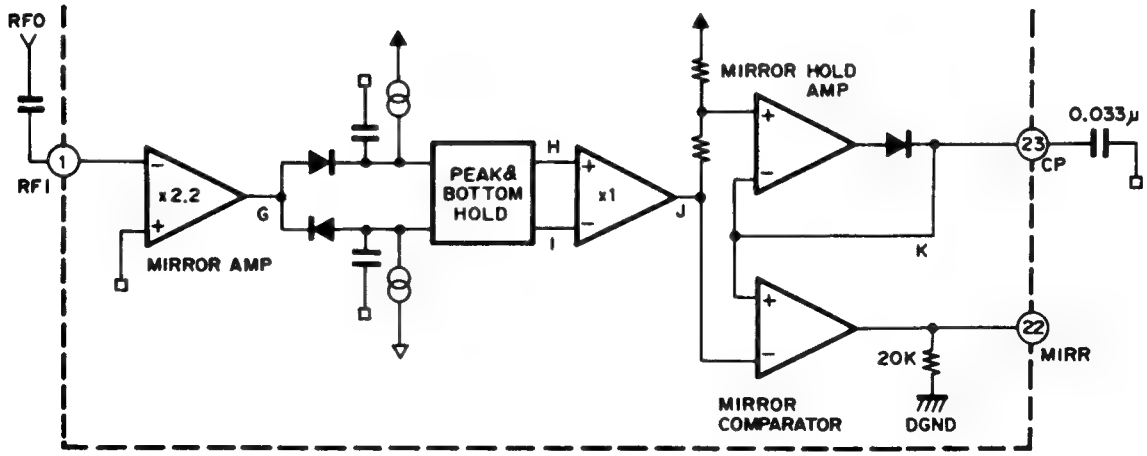
CIRCUIT DESCRIPTION

Mirror circuit

In the mirror circuit, after the RFI signal is amplified, both its peak and bottom are held.

While the peak hold is held by a time constant which can follow a traverse of 30 kHz, the bottom hold is held by a time constant which can follow a cyclic period envelope variation.



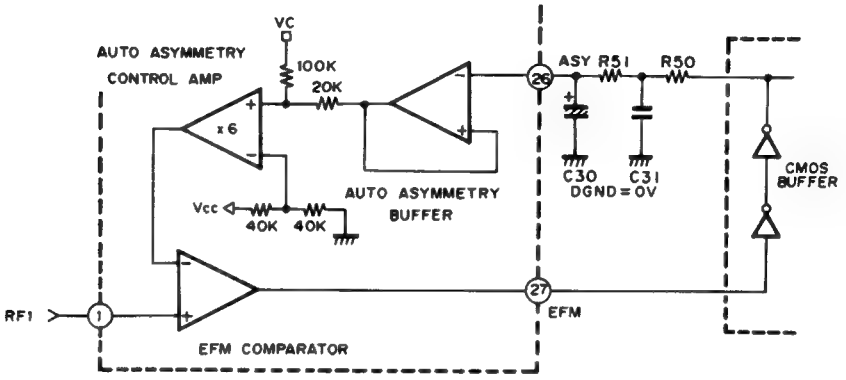


These peak and bottom hold signals, H and I are differentially amplified to obtain the DC-reproduced envelope signal J. This signal is compared with signal K, which is obtained by a peak hold with a large time constant corresponding to 2/3 of the peak value, so that the mirror output is obtained. That is, the mirror output goes "L" on the disc tracks and goes "H" between tracks (mirror section). In addition, the output goes "H" when a defect is detected. The time constant of the mirror hold should be quite large when compared with the traverse signal.

CIRCUIT DESCRIPTION

EFM comparator

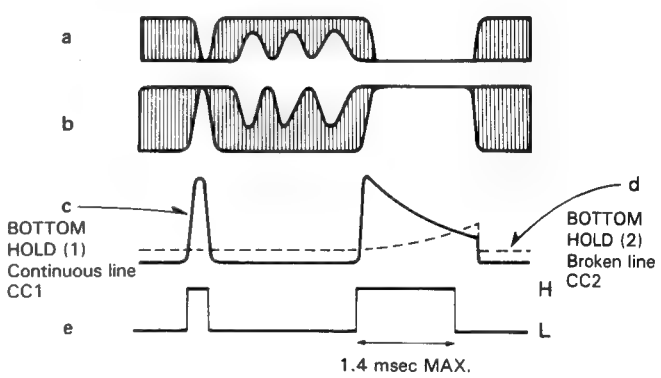
The EFM comparator converts the RF signal into a binary coded signal. Since asymmetry caused by dispersion when manufacturing the discs cannot be reduced by AC coupling only, the reference voltage of the EFM comparator is controlled using the characteristic that the present probability of a 1 or 0 is 50% each for the binary coded EFM signal.

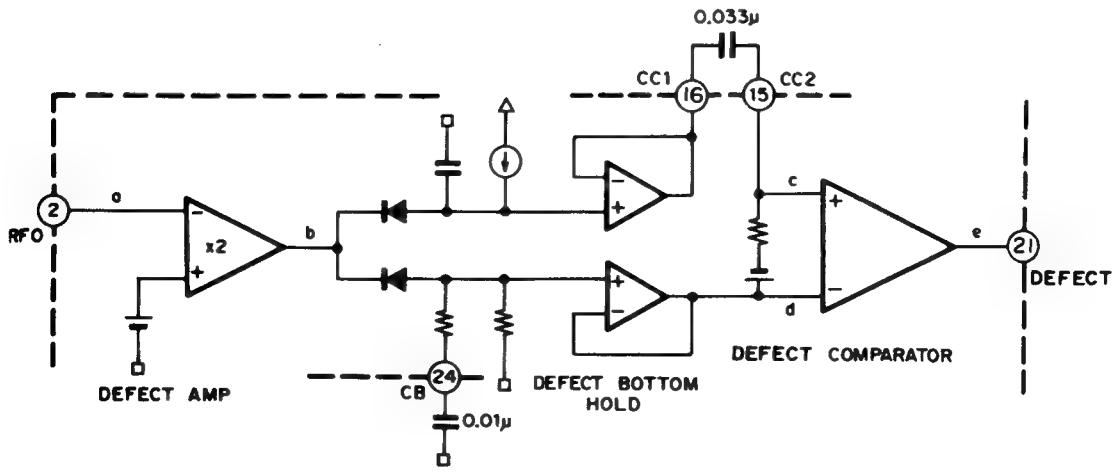


The EFM comparator is designed as a current switching type, and the "H" and "L" levels are not equal to the power voltages. Therefore, feedback is required via a CMOS buffer. R8, R9, C8 and C9 constitute an LPF to obtain the DC component of (Vcc + DGND)/2 (V). If the cut-off frequency (fc) is set to more than 500 Hz, leakage of the EFM low frequency signals will be greatly increased and will result in a degradation of the block error rate.

Defect circuit

After inverting the RFI signal, the defect circuit bottom holds with two long/short time constants. The bottom hold with a shorter time constant responds to a mirror defect of more than 0.1 msec on the disc, and the bottom hold with a longer time constant holds the mirror level obtained immediately before the defective section. These signals are C-coupled, then differentiated with level shifting. The signals are compared with each other to generate the mirror defect detecting signals.





CIRCUIT DESCRIPTION

U301: SERVO SIGNAL PROCESSOR FOR THE CD (CXA1082Q)

General

The CXA1082Q is a bipolar IC developed for servo control in Compact Disc players.

Features

- Operates on a signal +5 V power supply as well as on a ±5 V dual-voltage power supply.
- Low power consumption (165 mW with ±5 V, 100 mW with +5 V).
- Same servo function as CX20108 (focusing, tracking, sled servo)
- Built-in auto sequencer.
- Built-in spindle servo LPF.
- Built-in loop filter and VCO for an EFM clock generating PLL.
- A minimum of external parts required.
- Sled overrun prevention circuit.
- Disc defect treatment circuit.
- Anti-shock circuit
- Linear motor feed for high-speed access.
- Shared use of a serial data bus with the CX23035 and CXD1135Q.
- The microprocessor and software both have upward compatibility with the CX20108.
- The pulse height of the focusing search, track jump, and sled kick can be set with externally connected resistors.

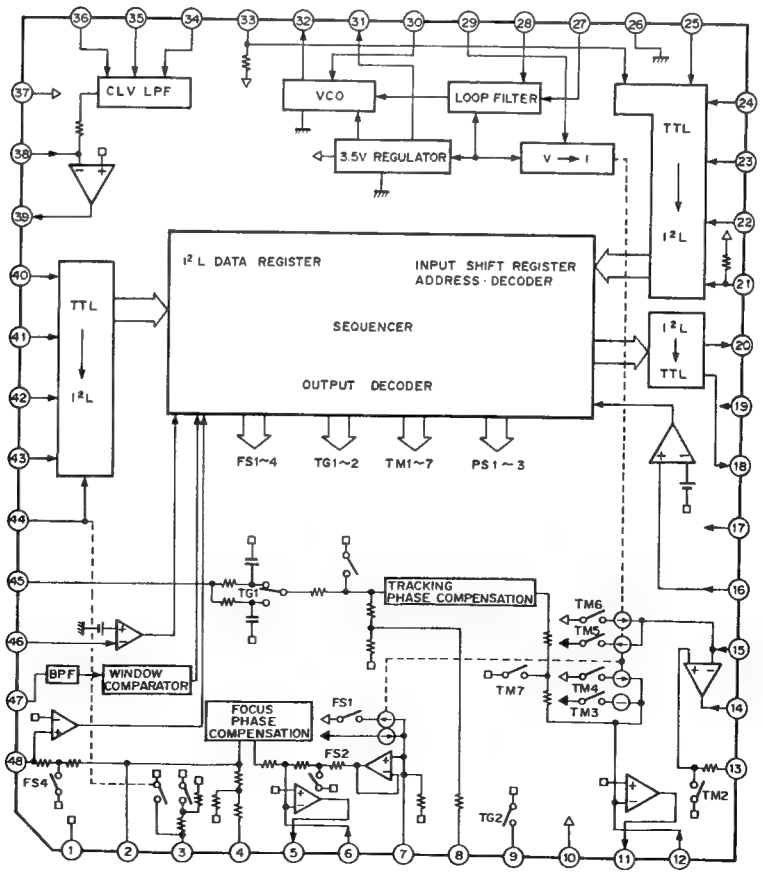
Functions

- Focusing servo control
- Tracking servo control
- Sled servo control
- Spindle servo
  Low Pass Filter, drive amplifier
- EFM clock generating PLL
  Loop filter: 8.64 MHz VCO
- Auto sequencer
  Incorporating a RAM

Structure

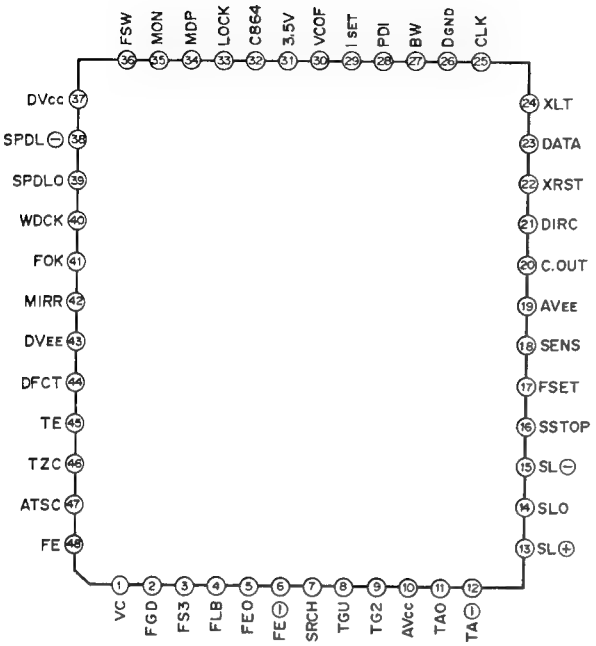
Bipolar silicon monolithic IC

Block diagram



CIRCUIT DESCRIPTION

Pin configuration

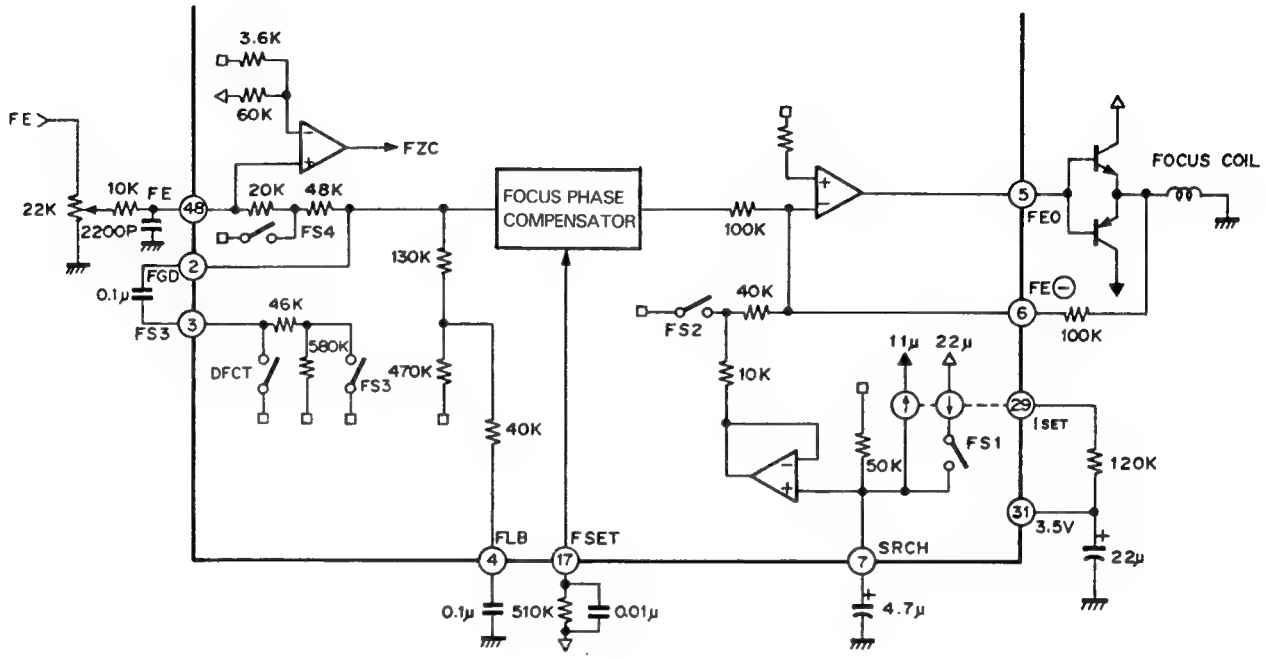


Terminal explanations

Terminal No.	Terminal name	Function
2	FGD	To lower the high frequency gain of the focus servo, insert a capacitor between this pin and pin 3.
3	FS3	The high frequency gain of the focus servo is selected by switching FS3 ON/OFF.
4	FLB	Time constant external connect pin, for boosting the focus servo low frequencies.
5 11 14 39	FEO TAO SLO SPDLO	Power transistor drive op amplifier output pins.
6	FE⊖	Focus amplifier inverted input pin.
7	SRCH	Time constant external connect pin, for creating the focus search waveform.
8	TGU	Time constant external connect pin, for selecting the tracking high frequency gain.
9	TG2	Time constant external connect pin, for selecting the tracking high frequency gain.
12	TA⊖	Tracking amplifier inverted input pin.
13	SL⊕	Sled amplifier non-inverted input pin.
15	SL⊖	Sled amplifier inverted input pin.
16	SSTOP	Limit switch ON/OFF detection signal input pin, for detecting the innermost edge of the disc.
17	FSET	Setting pin for the focus tracking phase peak value compensation, and fo of the CLV LPF.
18 20	SENS C.OUT	Output pins for an interface with a microprocessor.
21 22 23 24 25 33	DIRCT XRST DATA XLT CLK LOCK	Input pins for an interface with a microprocessor. A 47-kohm pull-up resistor is only incorporated in pins 21 and 33.
27	BW	Loop filter time constant external connect pin.
28	PDI	Input pin for the phase comparator output PDO of CXD23035/CXD1135.
29	ISET	Inputs a current which determines the level of the focus search, track jump, and sled kick.
30	VCOF	The self-advancing frequency of the VCO is almost proportional to the resistance between this pin and pin 31.
32	C864	8.64 MHz VCO output pin.
34	MDP	CXD23035/CXD1135 MDP pin connect pin.
35	MON	CXD23035/CXD1135 MON pin connect pin.
36	FSW	LPF time constant external connect pin, for the CLV servo error signal.
38	SPDL⊖	Spindle drive amplifier inverted input pin.
40 41 42 44	WDCK FOK MIRR DFCT	Input pins for an interface with a microprocessor.
45	TE	Tracking error signal input pin.
46	TZC	Tracking zero-cross comparator input pin.
47	ATSC	Window comparator input pin for ATSC detection.
48	FE	Focusing error signal input pin.

CIRCUIT DESCRIPTION

Focusing servo system



This block diagram is of the focusing servo system.

When FS3 is ON, the capacitor connected between pins 2 and 3 and the internal resistance determines the low-frequency time constant which can attenuate the high-frequency gain.

The capacitor between pin 4 and GND determines the time constant for boosting the low frequencies in normal playback.

The peak frequency of the focusing phase compensation is inversely proportional to the resistance connected to pin 17, and the frequency is about 1.2 kHz when the resistance is 510 k-ohms.

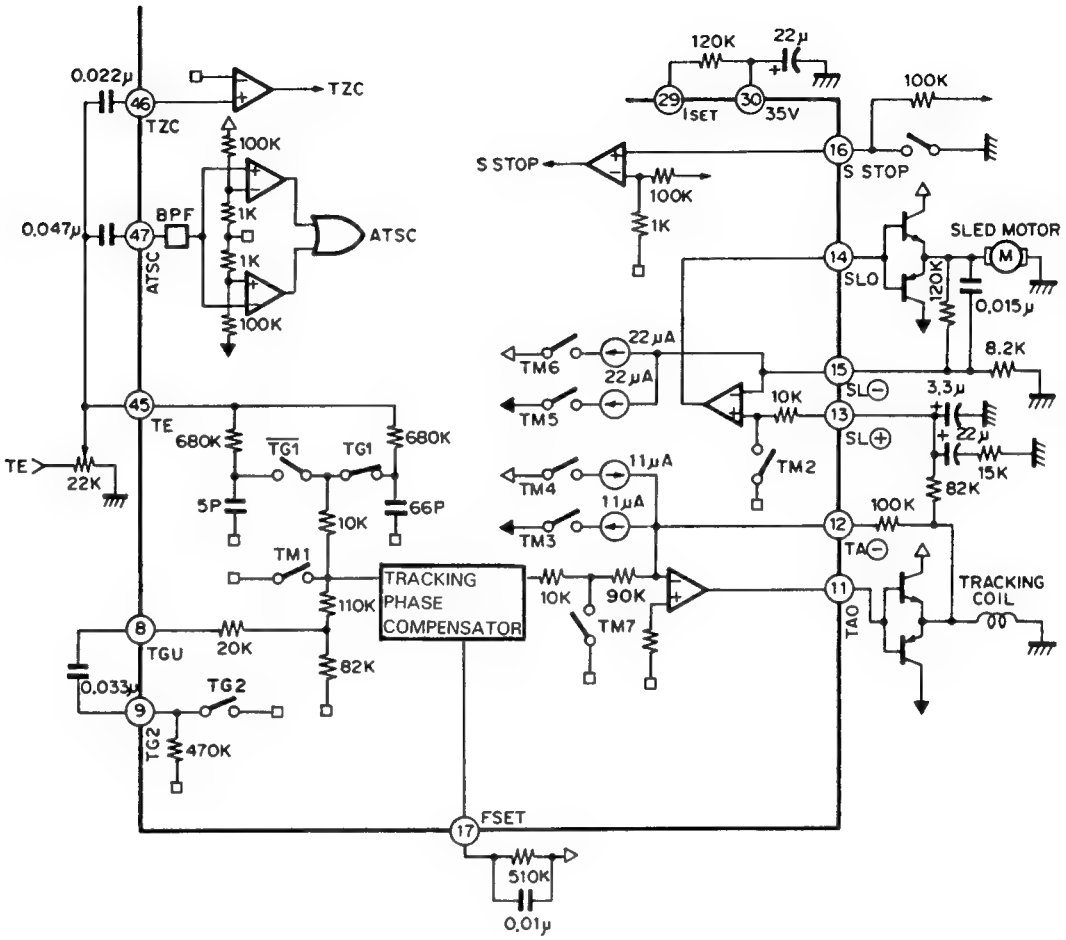
The focus search level is about ±1.1 Vp-p with these constants. The level is inversely proportional to the value of the resistance connected between pins 29 and 30. Note that the track jump and sled kick levels are also varied by changing this resistance.

The level has been set to 5.7% of the difference between Vcc, the inverted input reference voltage of the FZC comparator, and VC (pin 1); i.e. (Vcc−VC)×5.7%.

* Varying the value of resistance connected to pin 17 also varies the phase compensation peak values of focusing/tracking/sled servos and fc of the CVL LPF. At the same time, the op amplifier's dynamic range and offset voltage are also varied.

CIRCUIT DESCRIPTION

Tracking and sled servo system



This block diagram is of the tracking and sled servo system. The capacitor connected between pins 8 and 9 determines the time constant for attenuating the high-frequency gain. The peak frequency for the tracking phase compensation is inversely proportional to the resistance connected to pin 17, and the frequency is about 1.2 kHz when the resistance is 510 k-ohms.

A FWD or REV tracking jump is performed by switching TM3 or TM4 ON. At this time, the peak voltage applied to the tracking coil depends on the current at TM3 or TM4 and the feedback resistance through pin 12, as shown by the following equation:

Track jump peak voltage = TM3 (TM4) current × Feedback resistance

A FWD or REV sled kick is performed by switching TM5 or TM6 ON. At this time, the peak voltage applied to the sled motor depends on the current at TM5 or TM6 and the feedback resistance through pin 15, as shown by the following equation.

Sled jump peak voltage = TM5 (TM6) current × Feedback resistance

The currents at these switches are determined by the resistance connected between pins 29 and 31. When the value is 120 k-ohms, the currents are:

±11 μA at TM3 and TM4, and

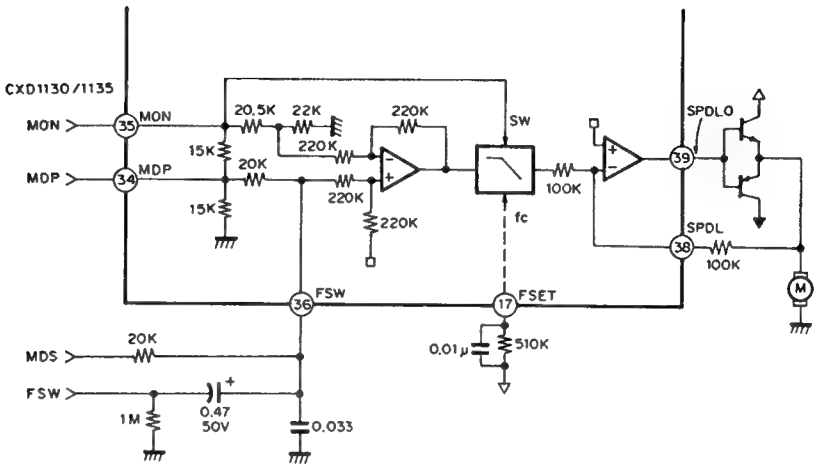
±22 μA at TM5 and TM6.

The currents are inversely proportional to the resistance, and the variable range is from about 5 to 40 μA with TM3.

S STOP is the signal used to detect the ON/OFF of the limit switch for detecting the innermost position for the linear motor.

CIRCUIT DESCRIPTION

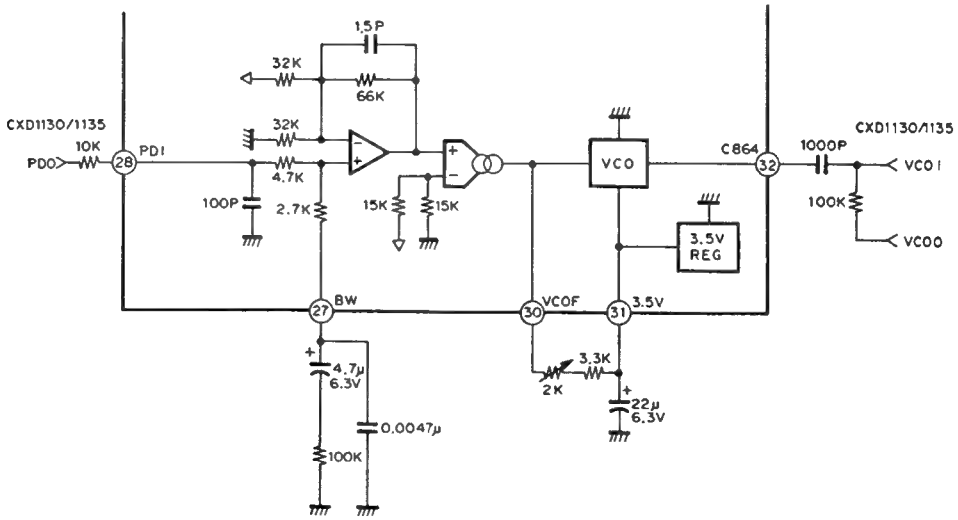
Spindle servo and LPF circuitry



The carrier component in the CLV servo error signals MDS and MDP are eliminated by a two-stage LPF, which consists of a 200 Hz LPF formed by a 0.033 μF capacitor and a 20 k-ohms resistor connected to pin 36 and an internal LPF (fc up to 200 Hz when 510 k-ohms is connected to pin 17).

In the CLV-S mode, FSW becomes L, and fc of the LPF at pin 36 drops to enhance the filtering effect. The resistor connected to pin 17 need not be stabilized but only connected to Vcc, because its fc will not be varied by supply voltage variation.

VCO loop filter and 8.64 MHz VCO circuitry



The phase comparator output, PDO, is input via pin 28, sent through the loop filter to eliminate the PWM carrier component, then V-I converted, and added with the self-advancing frequency set current from pin 30 for use in controlling the VCO frequency. The VCO's self-advancing frequency is almost proportional to the resistance connected between pins 30 and 31. The value of this resistance is set so that the PLL capture range center is 4.3218 MHz at CXD1135/1130 pin 70. The external circuit connected to pin 27 BW is used to maximize the capture range during accessing, so that access is possible even when the self-advancing frequency deviates due to the VCO's temperature characteristic, etc.

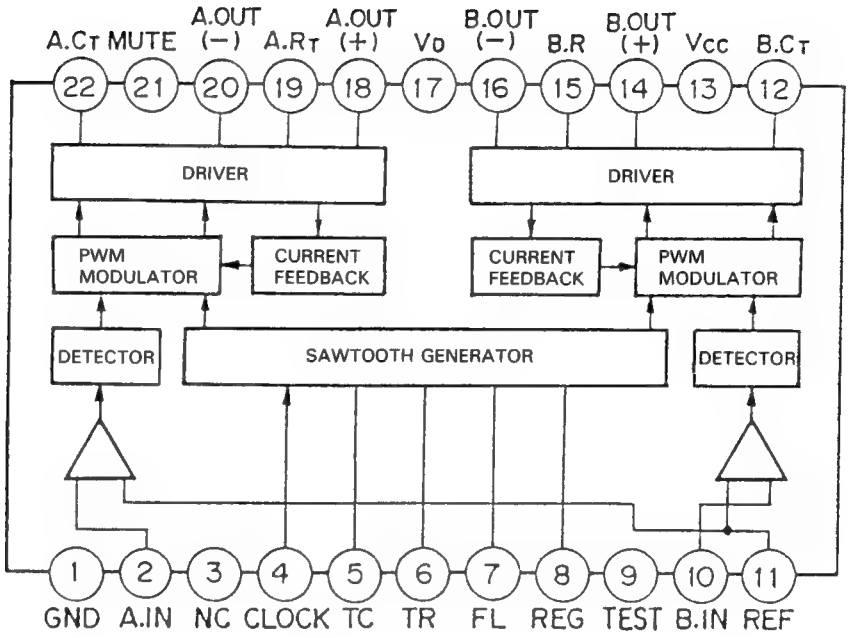
CIRCUIT DESCRIPTION

U351, U352: PWM DRIVERS FOR THE CD (BA6280AF)

Structure

Bipolar silicon monolithic IC

Block diagram



CIRCUIT DESCRIPTION

U401: DIGITAL SIGNAL PROCESSING LSI FOR THE CD (CXD1125Q)

General

The CXD1125Q is a digital signal processing LSI for a Compact Disc player, and has the following functions.

1. Bit clock reproduction by an EFM-PLL circuit
2. EFM data demodulation
3. Frame sync signal detection, protection and insertion
4. Powerful error detection and correction
5. Interpolation with an average value, or by holding the previous value
6. Demodulation of a sub code signal, error detection of a sub code Q
7. Spindle motor CLV servo
8. 8-bit tracking counter
9. CPU interface with a serial bus
10. Sub code Q register
11. Output to digital audio interface

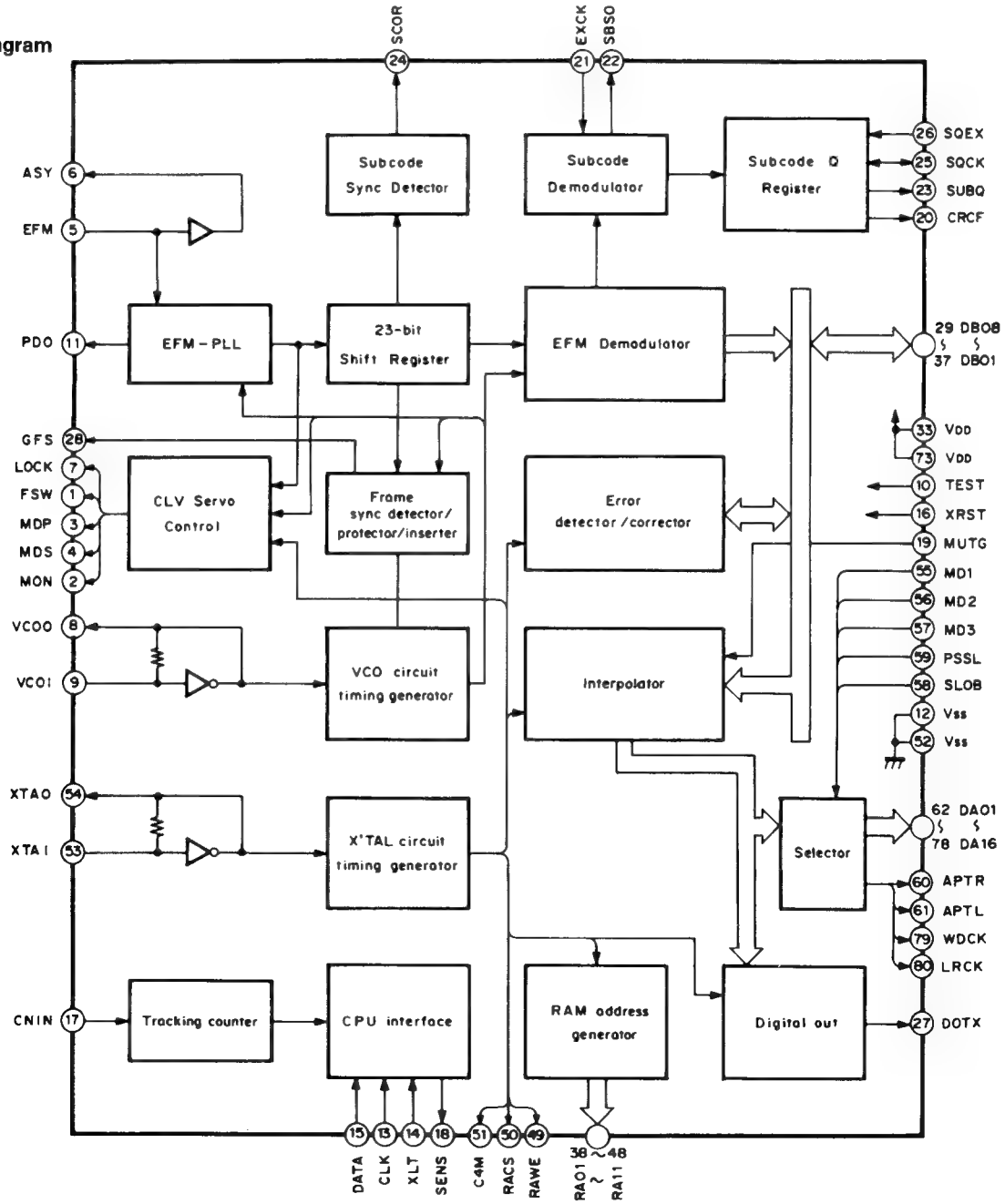
Features

- All digital signals used in playback can be processed using only a single chip.
- Digital audio interface output circuit

Structure

CMOS IC

Block diagram



CIRCUIT DESCRIPTION

Terminal explanations

Terminal No.	Terminal name	I/O	Function
1	FSW	O	Time constant switching output of output filter of spindle motor.
2	MON	O	ON/OFF control output of spindle motor.
3	MDP	O	Drive output of spindle motor. Rough speed control in CLV-S mode and phase control in CLV-P mode.
4	MDS	O	Drive output of spindle motor. Speed control in CLV-P mode.
5	EFM	I	EFM signal input from RF amplifier.
6	ASY	O	Output for controlling the slice level of EFM signal.
7	LOCK	O	Samples the GFS signal with WFCK/16, and outputs "H" when the level is high. When it is "L" for eight times, in arrow, outputs "L".
8	VCOO	O	VCO output. f=8.6436 MHz when locked to EFM signal.
9	VCOI	I	VCO input.
10	TEST	I	(0 V)
11	PDO	O	Phase comparison output of EFM signal and VCO/2.
12	V_{SS}	—	GND (0 V)
13	CLK	I	Serial data transmission clock input from CPU. Data is latched at rising edge of a clock.
14	XLT	I	Latch input from CPU. Data (serial data from CPU) from the 8 bit shift register is latched in each register.
15	DATA	I	Serial data input from CPU.
16	XRST	I	System reset input. Reset at "L".
17	CNIN	I	Input of tracking pulse.
18	SENS	O	Output of internal status in correspondence to the address.
19	MUTG	I	Muting input. In the case when ATTM of internal register A is "L". Normal status when MUTG is "L" or soundless state when it is "H".
20	CRCF	O	Output of result of CRC check of sub code Q.
21	EXCK	I	Clock input for sub code serial output.
22	SBSO	O	Sub code serial output.
23	SUBQ	O	Sub code Q output.
24	SCOR	O	Sub code sync S0+S1 output.
25	SQCK	I/O	Sub code Q read-off clock.
26	SQEX	I	SQCK select input.
27	DOTX	O	DIGITAL OUT output.
28	GFS	O	Display output of frame sync lock status.
29	DB08	I/O	Data pin of external RAM. DATA8 (MSB)
30	DB07	I/O	Data pin of external RAM. DATA7
31	DB06	I/O	Data pin of external RAM. DATA6
32	DB05	I/O	Data pin of external RAM. DATA5
33	V_{DD}	—	Power supply (+5 V)
34	DB04	I/O	Data pin of external RAM. DATA4
35	DB03	I/O	Data pin of external RAM. DATA3
36	DB02	I/O	Data pin of external RAM. DATA2
37	DB01	I/O	Data pin of external RAM. DATA1 (LSB)
38	RA01	O	Address output of external RAM. ADDR01 (LSB)
39	RA02	O	Address output of external RAM. ADDR02
40	RA03	O	Address output of external RAM. ADDR03
41	RA04	O	Address output of external RAM. ADDR04
42	RA05	O	Address output of external RAM. ADDR05
43	RA06	O	Address output of external RAM. ADDR06

CIRCUIT DESCRIPTION

Terminal No.	Terminal name	I/O	Function
44	RA07	O	Address output of external RAM. ADDR07
45	RA08	O	Address output of external RAM. ADDR08
46	RA09	O	Address output of external RAM. ADDR09
47	RA10	O	Address output of external RAM. ADDR10
48	RA11	O	Address output of external RAM. ADDR11 (MSB)
49	RAWE	O	Write Enable signal output to external RAM. (Active at "L").
50	RACS	O	Chip select signal output to external RAM. (Active at "L").
51	C4M	O	Crystal dividing output. f= 4.2336 MHz.
52	V_{SS}	—	GND (0 V).
53	XTAI	I	Crystal oscillator input. (16.9344 MHz)
54	XTAO	O	Crystal oscillator output. (16.9344 MHz)
55	MD1	I	Mode select input 1.
56	MD2	I	Mode select input 2.
57	MD3	I	Mode select input 3.
58	SLOB	I	Audio data output code select input. 2's complement output when "L", offset binary output when "H".
59	PSSL	I	Audio data output mode select input. Serial output when "L", parallel output when "H".
60	APTR	O	Aperture compensation control output. "H" when R-ch.
61	APTL	O	Aperture compensation control output. "H" when L-ch.
62	DA01	O	DA01 (parallel audio data LSB) output when PSSL="H", C1F1 output when PSSL="L".
63	DA02	O	DA02 output when PSSL="H", C1F2 output when PSSL="L".
64	DA03	O	DA03 output when PSSL="H", C2F1 output when PSSL="L".
65	DA04	O	DA04 output when PSSL="H", C2F2 output when PSSL="L".
66	DA05	O	DA05 output when PSSL="H", C2FL output when PSSL="L".
67	DA06	O	DA06 output when PSSL="H", C2PO output when PSSL="L".
68	DA07	O	DA07 output when PSSL="H", RFCK output when PSSL="L".
69	DA08	O	DA08 output when PSSL="H", WFCK output when PSSL="L".
70	DA09	O	DA09 output when PSSL="H", $\overline{\text{PLCK}}$ output when PSSL="L".
71	DA10	O	DA10 output when PSSL="H", UGFS output when PSSL="L".
72	DA11	O	DA11 output when PSSL="H", GTOP output when PSSL="L".
73	V_{DD}	—	Power supply (+5 V).
74	DA12	O	DA12 output when PSSL="H", RAOV output when PSSL="L".
75	DA13	O	DA13 output when PSSL="H", C4LR output when PSSL = "L".
76	DA14	O	DA14 output when PSSL="H", $\overline{\text{C21O}}$ output when PSSL="L".
77	DA15	O	DA15 output when PSSL="H", C21O output when PSSL="L".
78	DA16	O	DA16 (parallel audio data MSB) output when PSSL="H", DATA output when PSSL="L".
79	WDCK	O	Strobe signal output. (88.2 kHz)
80	LRCK	O	Strobe signal output. (44.1 kHz)

Notes:

C1F1 :
C1F2 : Error correction status monitor output for C1 decode.

C2F1 :
C2F2 : Error correction status monitor output for C2 decode.

C2FL : Correction status output. Goes "H" when the currently corrected C2 series data cannot be corrected.

C2PO : C2 pointer signal. Synchronized to the audio data output.

RFCK : Read frame clock output. 7.35 MHz when locked to the crystal line.

WFCK: Write frame clock output. 7.35 MHz when locked to the crystal line.

$\overline{\text{PLCK}}$: VCO/2 output. f=4.3218 MHz when locked to the EFM signal.

UGFS : Non-protected frame sync pattern output.

GTOP : Frame sync protect status display output.

RAOV : ±4 frame jitter absorption RAM overflow and underflow display output.

C4LR : Strobe signal. (176.4 kHz)

$\overline{\text{C21O}}$: C21O invert output.

C21O : Bit clock output. (2.1168 MHz)

DATA : Audio signal serial data output.

CIRCUIT DESCRIPTION

Explanation of functions

1. CPU interface

(1) Data input

Each register may be set by input of 4-bit address, and 4-bit data from LSB in the timing that is shown in Fig. 1 to three pins, XLT, CLK and DATA. The address and data of each pin are as shown in Table 1, and their functions are as follows. The contents of each register become entirely 0 when XRST = "L".

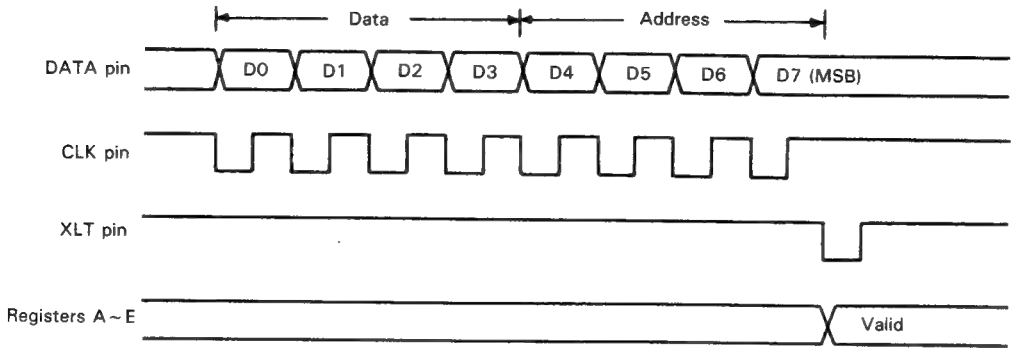


Fig. 1 Timing chart for data input

(2) Registers

Register 9 — New function control

Controls the new functions address to the CX23035.

D0 : CRCQ — Switches ON/OFF the function which outputs the CRCF data to the SUBQ pin from the rising edge of SCOR to the trailing edge of SQCK. Details are described in "**1-(5). Subcode output**". (Page 34)

D1 : NCLV — Switches between the old CLV-P servo and the new CLV-P servo by comparison with newly added base counter. Details are described in "**6. CLV servo control**". (Page 40)

D2 : HZPD — One of the defect countermeasures. Switches ON/OFF the function which makes the PDO pin a high impedance (Z) for a maximum of 0.55 ms from the trailing edge of GFS. Details are described in "**10. Countermeasures to defects**". (Page 47)

D3 : ZCMT — Switches the zero cross mute function ON/OFF. Details are described in "**7. Interpolation and mute, attenuate**". (Page 45)

Register A — Sync. protection, attenuator control

D0 : ATTM — Used for attenuating audio signals by 12 dB.

D1 : WSEL — Provided for switching frame sync. protection characteristics in correspondence to the time of playback and time of access. Details will be described in the paragraph of "**2. EFM demodulation**". (Page 36)

D2 : GSEL

D3 : GSEM

Registers B and C — Counter set, more significant 4-bit (register C) and less significant 4-bit (register B)

These registers are used for setting the tracking counter value. The data of registers B and C are preset in the counter through the 4-bit buffer register assigned by address.

Accordingly, when data of either register B or C is input, the contents of both registers are preset in the counter simultaneously as 8-bit data (either buffer register is of "OLD" data).

Register D-CLV control

D0 : GAIN — Used for setting the gain of MDP pin output in the CLV-S and CLV-H modes. It is −12 dB (time of 3/4 out of the period of RFCK/2 is of high impedance) when D0 = 0 or is 0 dB when D0 = 1.

D1 : T_P — Used for setting the period of peak hold in the CLV-S mode. Peak hold is made in the period of RFCK/4 when D1 = 0 or in the period of RFCK/2 when D1 = 1.

D2 : T_B — Used for determining the period of bottom hold in the CLV-S and CLV-H modes. Bottom hold is made in the period of RFCK/32 when D2 = 0 or in the period of RFCK/16 when D2 = 1.

D3 : DIV — Used for setting the frequency dividing ratio of RFCK, WFCK in the CLV-P mode. When D3 = 0, phase comparison of RFCK/4 and WFCK/4 is made, and output is made out of MDP pin in each case.

CIRCUIT DESCRIPTION

Register E — CLV mode

It is as shown in Table 1.

The details of each mode will be described in "**6. CLV servo control**". (Page 37)

D3 to D0 are all "0" when XRST = L.

Register name	Command	Address D7 ~ D4	Data				SENS pin
			D3	D2	D1	D0	
9*1	New function control	1001	ZCMT	HZPD	NCLV	CRCO	Z
A*2	Sync protection attenuator control	1010	GSEM	GSEL	WSEL	ATTM	Z
B	Counter set, Less significant 4-bit	1011	Tc3	Tc2	Tc1	Tc0	$\overline{\text{COMPLETE}}$
C	Counter set, More significant 4-bit	1100	Tc7	Tc6	Tc5	Tc4	$\overline{\text{COUNT}}$
D*3	CLV control	1101	DIV	T_B	T_P	GAIN	Z
E*4	CLV mode	1110	CLV mode				$\overline{\text{PW} \geqq 64}$

***1 Register 9**

		Dn = 0	Dn = 1
ZCMT	D3	Zero-cross MUTE off	Zero-cross MUTE on
HZPD	D2	PDO pin is always active.	PDO pin is "Z" at the trailing edge of GFS.
NCLV	D1	CLV-P servo for the frame sync signal	CLV-P servo for the base counter
CRCQ	D0	CRCF is not superimposed on SUBQ	SUBQ = CRCF at the raising edge of SCOR

***2 Register A**

GSEM	GSEL	Frame
0	0	2
0	1	4
1	0	8
1	1	13

WSEL	Clock
0	±3
1	±7

ATTM	MUTG pin	dB
0	0	0
0	1	$-\infty$
1	0	−12
1	1	−12

***3 Register D**

DIV	D3	0	RFCK/4, WFCK/4	Phase comparison frequency in CLV-P mode
		1	RFCK/8, WFCK/8	
T_B	D2	0	RFCK/32	Bottom hold period in CLV-S, CLV-H mode
		1	RFCK/16	
T_P	D1	0	RFCK/4	Peak hold frequency in CLV-S mode
		1	RFCK/2	
GAIN	D0	0	−12 dB	Gain at MDP pin in CLV-S, CLV-H mode
		1	0 dB	

***4 Register E**

Mode	D3 ~ D0	MDP pin	MDS pin	FSW pin	MON pin
STOP	0000	L	Z	L	L
KICK	1000	H	Z	L	H
BRAKE	1010	L	Z	L	H
CLV-S	1110	CLV-S	Z	L	H
CLV-H	1100	CLV-H	Z	L	H
CLV-P	1111	CLV-P	CLV-P	Z	H
CLV-A	0110	CLV-S or CLV-P	Z or CLV-P	L or Z	H

Z: High impedance

Table 1 List of registers

CIRCUIT DESCRIPTION

(3) Tracking counter

This counter is provided for facilitating track jump. Load the number of tracks to be jumped in registers B and C. Count of CNIN pulses is started at rising edge of XLT after it was loaded in either register B or C.

When n (n = 256 is meant when register B = register C = 0) is loaded in registers and the address is set at "B", a signal ($\overline{\text{COMPLETE}}$) that is of HIGH level up to "n" pulses and is of LOW level after "n" pulses is output of SENS pin. When the address is set at "C", signal ($\overline{\text{COUNT}}$) of CNIN/2n (Hz) is output.

The tracking counter timing chart is shown in Fig. 2.

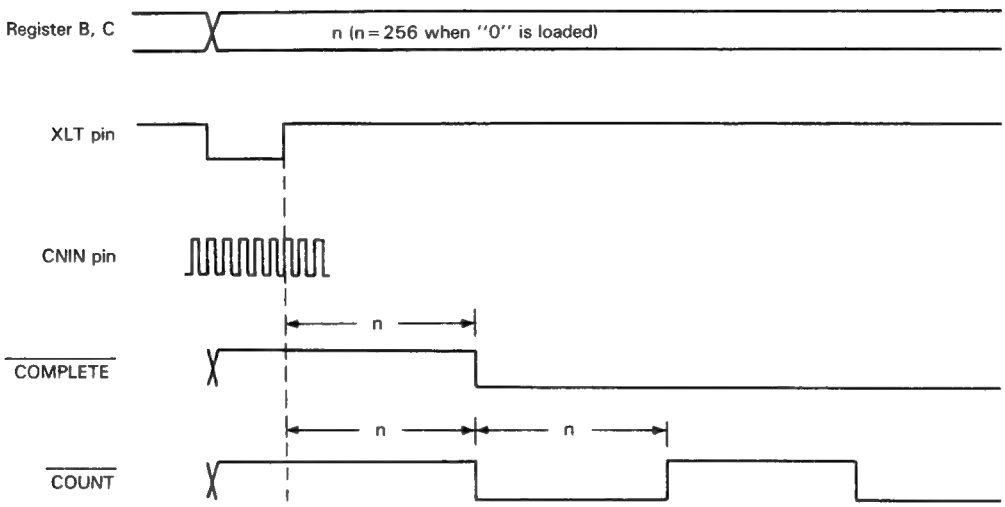


Fig. 2 Tracking counter timing chart

(4) SENS

The following signals are output from SENS pin depending on the address of D7 ~ D4.

(1) $\overline{\text{COMPLETE}}$: Address (see note) is "B"; Shown in Fig. 2.

(2) $\overline{\text{COUNT}}$: Address (see note) is "C"; Shown in Fig. 2.

(3) $\overline{\text{PW} \geqq 64}$: Address (see note) is "E"; This signal is of LOW level when the pulse width after bottom hold is over 63, and is of HIGH level otherwise. It is used for detection of a drop in the speed of the spindle motor after braking and so on.

Note: Address setting is determined by the data corresponding to D4 to D7, which are input from the DATA pins shown in Fig. 1.

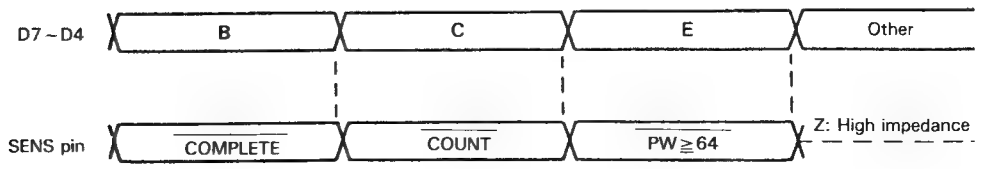


Fig. 3 Timing chart of SENS pin

CIRCUIT DESCRIPTION

(5) Sub code output

Sub codes P ~ W loaded in the 8-bit shift register are output out of SBSO pin in accordance with the clock input through EXCK pin. When SCOR pin is "H", S0 + S1 signal is output. Sub code Q is as follows, depending on the SQEX pin status.

a. When the SQEX pin is "L", sub code Q is output from the SUBQ pin in synchronism with the WFCK signal in the same way as for the CX23035. The $\overline{\text{WFCK}}$ is also output from the SQCK pin.

b. When the SQEX pin is "H", sub code Q is output from the SUBQ pin in synchronism with the external clock (as from the microprocessor). Two 80-bit shift registers, for reading and writing, are incorporated as shown in Fig. 7, and while the microprocessor reads, the new sub code Q is written to another register. The microprocessor is interrupted from the outside at the rising edge of the SCOR pin, and after checking the CRCF flag (output to the CRCF pin, or the SUBQ pin when the CRCQ flag is "1"), the CRCF is checked. If CRCF = "H", a shift lock is output and the new sub code Q is read. After the LSB side is replaced with the MSB side by a unit of 4-bit, the data is stored in register. As the microprocessor serially inputs from the LSB first, replacing the 4-bit of data is unnecessary.

(a) Timing of SBSO, SUBQ, SCOR, CRCF

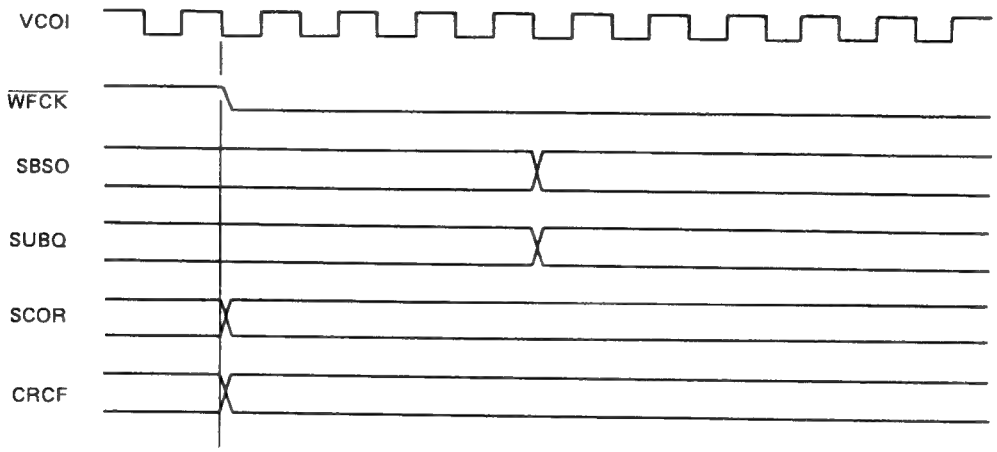
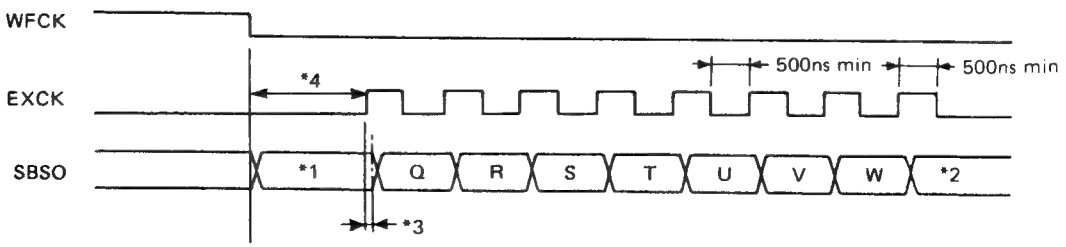


Fig. 4

(b) Timing of SBSO, EXCK



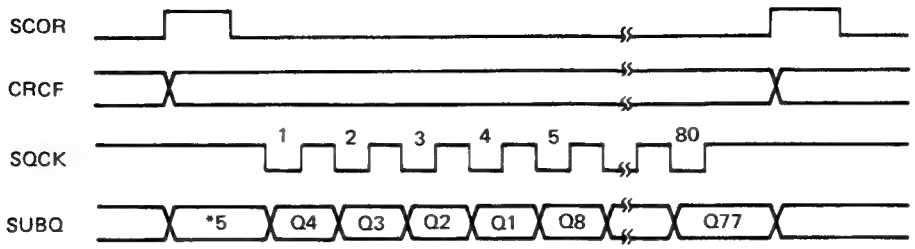
*1: Sub code P is output when SCOR is 0.
S0 + S1 is output when SCOR is 1.
*2: SBSO is 0 when 8 or more pulses are input to EXCK.
*3: 4T ~ 6T if the period of VCO is expressed as T.
*4: Make EXCK low for 10 μs from the rising edge of WFCK.
One time period of T = 8.6436 MHz.

Fig. 5 Timing chart of sub code outputs

CIRCUIT DESCRIPTION

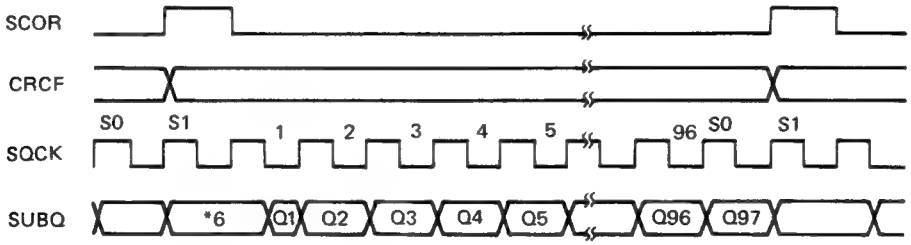
(c) Timing of SCOR, CRCF, SQCK, SUBQ

SQEX = "H" level



*5: CRCF when CRCQ flag is "1", undefined when "0".

SQEX = "L" level



*6: CRCF when CRCQ flag is "1", Q98, Q1 when "0".

Fig. 6 Timing chart of sub code outputs

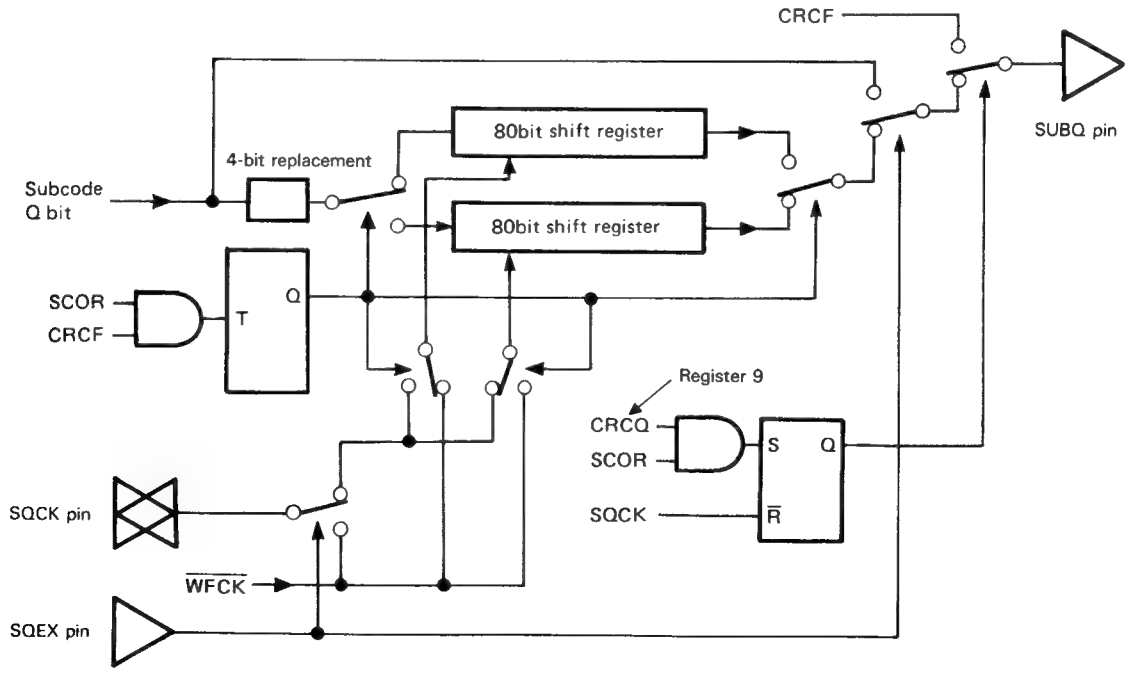


Fig. 7

CIRCUIT DESCRIPTION

2. EFM demodulation

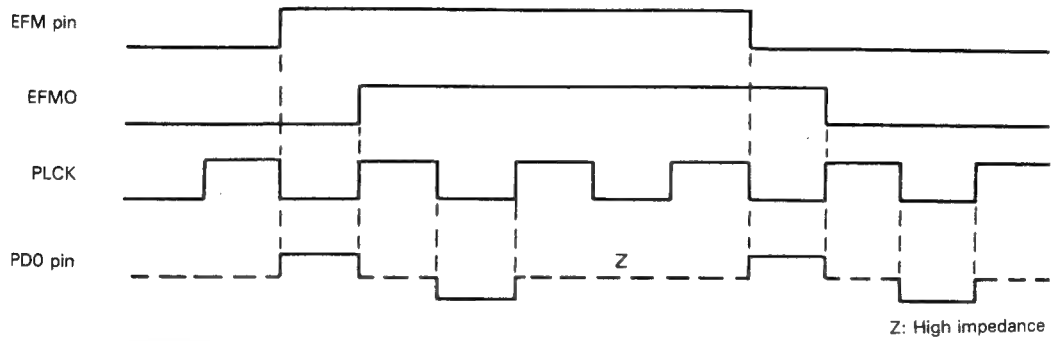
(1) Playback of bit clock by EFM-PLL circuit

The EFM signal read out of the optical block contains a clock component of 2.16 MHz. Therefore, it is possible to take out a bit clock (PLCK) of 4.32 MHz synchronized with this clock by the EFM-PLL circuit.

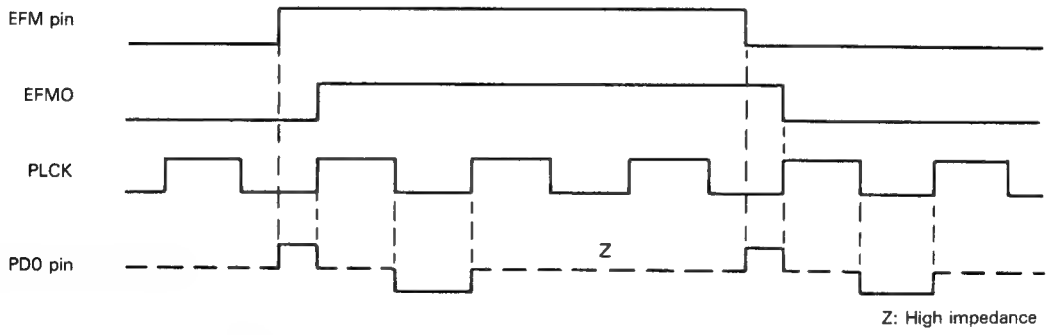
At each edge of EFM signal, phase comparison is made with PLCK, which is 1/2 of VCO, is made and output is made by TRI STATE out of PDO pin. The mean value of PDO pin is about 1/2 VDD if synchronized, but the mean value drops when VCO becomes higher. On the other hand, the mean value increases when VCO becomes less.

The timing charts of EFM pin, EFMO, PLCK and PDO are shown in Fig. 8.

(a) When EFM signal and VCO are synchronized



(b) When VCO is higher than EFM signal



(c) When VCO is less than EFM signal

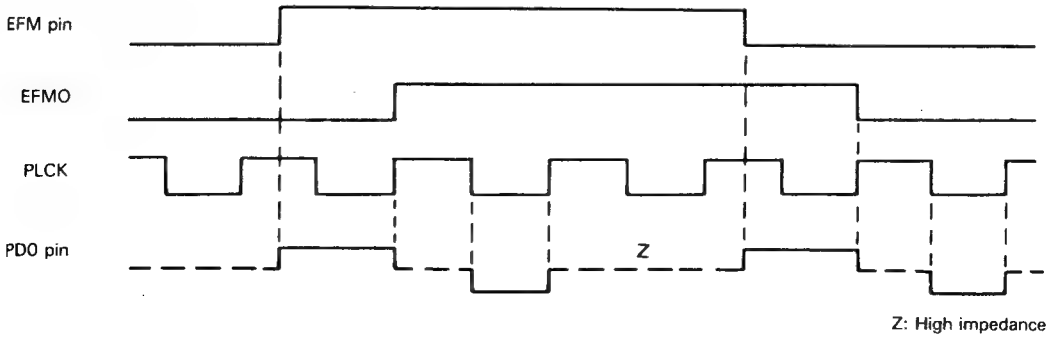


Fig. 8 Timing charts of EFM-PLL circuit

CIRCUIT DESCRIPTION

(2) Detection, protection and interpolation of frame synchronizing signals

There are cases during recording where the same pattern is detected in the data due to the influence of drop-out and jitter, even if a pattern that is same as the synchronizing signal will not appear.

On the other hand, there also are cases where original frame synchronizing signal is not detected. Therefore, protection and interpolation are required besides detection.

The edge portion only of EFM signal (EFMO) latched with PLCK is converted to "1" and the rest to "0", and then input is to a 23-bit shift register and a frame synchronizing signal is detected.

In order to protect a frame synchronizing signal, a window is provided and the same patterns outside of this window are removed. This width can be selected with WSEL.

If no frame synchronizing signal is located in this window, interpolation is made with a signal produced by 588-mal counter (4.3218 MHz/588 = 7.35 kHz)

A 4-bit counter for counting the number of these frames to be interpolated is provided, and when its count reaches the level selected with GSEL, GSEM, the window is ignored and the 4-bit counter is reset with the next frame synchronizing signal. The GTOP pin is of "H" while this operation is performed. Further, GSF pin is of "H" when the frame synchronizing signal generated by the 588-mal counter for making interpolation is synchronized with the frame synchronizing signal from the disc.

The frame synchronizing signal before passage through the window or the window is output out of UGFS (DA05 pin at the time when PSSL = L).

WSEL	Window width
0	±3 clock
1	±7 clock

GSEM	GSEL	Number of frame to be interpolated	UGFS (PSSL = L)
0	0	2 frames	Window
0	1	4 frames	Window
1	0	8 frames	Frame synchronizing signal before passage through window.
1	1	13 frames	Window

The timing for write request signal (WREQ). Write Frame Clock (WFCK), etc. is generated based on the protected and interpolated frame synchronizing signal.

(3) EFM demodulation

14-bit data is taken out of the 23-bit shift register and is demodulated to 8-bit data through 14 →8 conversion circuit composed of array logics. Then a write request (WREQ) signal is output to the RAM interface block, and the data is then output to the data bus (DB08 - DB01 pins) of the RAM in accordance with the OENB signal transmitted from said block.

3. Sub code demodulation

(1) Sub code demodulation

Synchronizing signals S0 and S1 of 14-bit sub codes are detected out of the 23-bit shift register, and sampling is made in the timing that is synchronized with WFCK.

After delay of S0 by one frame, S0 + S1 is output out of SCOR pin and S0 · S1 is output out of SBSO pin (only when SCOR = H).

Data (P - W) of sub codes only is input to the register in the timing synchronized with WFCK after EFM demodulation; and sub code Q is output out of SUBQ pin, and at the same time, it is loaded in the 8-bit shift register and is output out of SBSO pin in correspondence to a clock from EXCK pin.

The details of this timing will be shown in **"1, CPU interface"**. (Page 28)

(2) Sub code Q error detection

The CRC result of sub code Q is output from the CRCF pin in synchronism with the SCOR pin.

It goes "L" when an error is detected. If the CRCQ flag is "1" at this time, the CRCF flag is output from the SUBQ pin during the time from the rising edge of the SCOR pin to the trailing edge of the SUBQ pin. This timing is detailed in **"1. CPU interface"**.

CIRCUIT DESCRIPTION

4. RAM interface (generation of external RAM address)

(1) Request from EFM demodulation block (Write RAM request)

When one symbol of demodulation is complete in the EFM demodulation block requests to write data to the external RAM to the RAM interface block. This request is WREQ signal.

This block gives priority orders to requests from other blocks and processes these requests.

When EFM write request is received, an address is generated to the RAM and Write Enable state is produced. Furthermore, a data output instruction is issued against the EFM demodulation block. This instruction is OENB signal.

Clocks of PLL system are used for EFM block and for requests (WREQ) from EFM block, but clocks of X'tal system are used for processing thereafter.

(2) Request from D/A converter output circuit (Read to D/A request)

This is a de-interleaved data request issued out of the timing generator in this block.

This request is of the highest priority among all requests, and addresses of three types are generated against this request.

This request is generated once every 24 periods based on the period of system clock **C212 (8.4672 MHz/4)**. The data output out of the RAM is C2 pointer first, less significant 8-bit out of 16-bit and finally more significant 8-bit.

(3) Request from error correction block (C1/C2 correction, pointer R/W)

The error correction block requests the data located on the system (C1/C2) to be corrected. Furthermore, there is a request to rewrite incorrect data to correct data.

In addition, there is a request for pointer R/W which indicates reliability of data.

These requests are made by the 8-bit data directed to the RAM interface block from the error correction block.

The requests from the error correction unit are of the lowest priority among requests of three types.

After acceptance of a request, data from RAM is directed to the 3rd clock of C212.

The data of acceptance of a request is output to the error correction block as a PREN signal.

This block generates type address of the requested data, and controls R/W of the RAM at the same time.

(4) Address generation

The data after EFM demodulation is data subjected to interleave processing.

This interleave processing is subjected to data lag by the unit of a frame.

Data of 108 frames are required for de-interleave. In other words, for obtaining one frame of audio data played in a certain length of time, data of 108 frames after EFM demodulation are required. Further, the system data of C1/C2 is of the system in the process of application of interleave, and therefore, is included in 108 frames.

Data in practice are generated continuously. That is, de-interleave should be updated by the unit of a frame. Therefore, Read/Write base counters are required. This base counter performs counting by the unit of a frame.

The writer base counter is used only at the time of EFM data writer.

The address directed to the external RAM is determined by the relative lag value to EFM demodulation data and their number of frames.

(5) Priority of address generation request

The system control block determines priority of address generation requests made to the RAM interface block.

The priority order is as follows, beginning with higher priority.

1. Read to D/A request
2. Write to RAM request
3. C1/C2 request

The number of times of requests is as follows.

1. Requests of 12 times in the frame section
   The number of times of address generation to it is 36 times.
2. Requests of 32 times in the frame section
   The number of times of address generation to it is 32 times.
3. Maximum number of times of request (C1 Double error correction, C2 pointer copy)
   Read R/W 64 times, Point R/W 65 times in one frame section
   The number of times of address generation to it is 129 times.

CIRCUIT DESCRIPTION

288 C212 (clocks) are included in a frame, and the number of times of operation of the RAM in it is 197 times at maximum.
In the system control block, against request 1, the timing of its occurrence is reserved in advance. Requests 2, 3 are generated simultaneously, priority is given to request 2, and if a request is generated during execution of either request, priority is given to the job in execution.

(6) Jitter margin

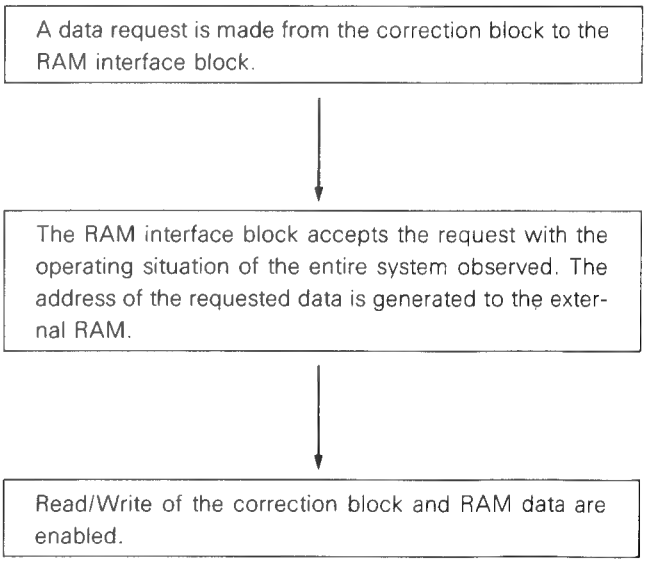
The EFM demodulation data is synchronized with data's playback system (PLL) as described earlier. Accordingly, it includes disturbance (wow, flutter, etc.) of disc rotation servo, etc. It is loaded to the external RAM. As the data taken out of the RAM is synchronized with the clock of X'tal system, this RAM is subjected to time axis correction.
However, the limit of time axis correction is determined by the capacity of the RAM. In this system, other data is destroyed when read/write frames are spaced apart by ±5 frames. In such a status how the playback sound is cannot be guaranteed. The base counter monitor is provided in order to avoid it.
In other words, when the difference between read base counter and write base counter exceeds ±4 frames, the write base counter is set in the value of the read base counter.
As a result, there is no case where data without error correction is output to the D/A.
The RAOV signal is of "H" for one frame (WFCK) section when the difference between base counters exceeded ±4 frames.

5. Error correction

(1) The error correction block makes correction up to double errors with each of C1 correction and C2 correction.
(2) This system adopts a unique pointer erasure method in order to minimize erroneous correction. Accordingly, the external 16K RAM stores these pointer data in addition to audio data.
(3) The pointer generated in C1 correction is called C1 pointer and the pointer generated in C2 correction is called C2 pointer.
(4) When the data of C1 system is judged as reliable, a C1 pointer is set in this system.
(5) During C2 correction, whether correction is to be made or not to be made and whether the data is reliable or unreliable are judged from the error location, locations and number of C1 pointers obtained through computation. A C2 pointer is set against an unreliable word (16-bit).
(6) The word in which a C2 pointer was set is subjected to previous value hold or mean value interpolation when it is output out of this LSI.
(7) Terminal C2FL becomes "H" when one or more C1 pointers are set in the data included in the C2 system at the time of C2 correction. C2FL is reset to "L" in minimum 472ns (see Note) after deactivation of pin RFCK. C2FL is the AND of C2F1 and C2F2.

Note: 472ns: One period of 2.1168 MHz

(8) The flow of data with the external RAM is as follows.



(9) When PSSL is set at "L", a signal that is capable of monitoring error correction is output.
C1F1, C1F2, C2F1 and C2F2 output to DA01 - DA04 are these monitor signals. These signals are reset to "L" when a period of minimum 472ns has elapsed since deactivation of RFCK.
The levels and meanings of these signals at the time of deactivation of RFCK are as follows.

CIRCUIT DESCRIPTION

C1F1	C1F2	C1 correction status
0	0	No error
1	0	Single error correction
0	1	Double error correction
1	1	Irretrievable error

C2F1	C2F2	C2FL	C2 correction status
0	0	0	No error
1	0	0	Single error correction
0	1	0	Double error correction
1	1	1	Irretrievable error

6. CLV servo control

The spindle motor revolution is controlled with one selected out of the following seven modes in accordance with a command from the CPU. CLV is the abbreviation of Constant Linear Velocity. The output is composed of MDP pin for controlling synchronization of velocity and phase, MDS pin for controlling synchronization of velocity, FSW pin for making selection of filter constant and MON pin for controlling motor ON/OFF.

(1) STOP: Register E = 0000'B (B means binary)
Mode for stopping the spindle motor.
MDP = FSW = MON = "L", MDS = "Z"

(2) KICK: Register E = 1000'B
Mode for running the spindle motor in forward direction.
MDP = MON = "H", MDS = "Z", FSW = "L".

(3) BRAKE: Register E = 1010'B
Mode for running the spindle motor in reverse direction.
MDP = FSW = "L", MDS = "Z", MON = "H".

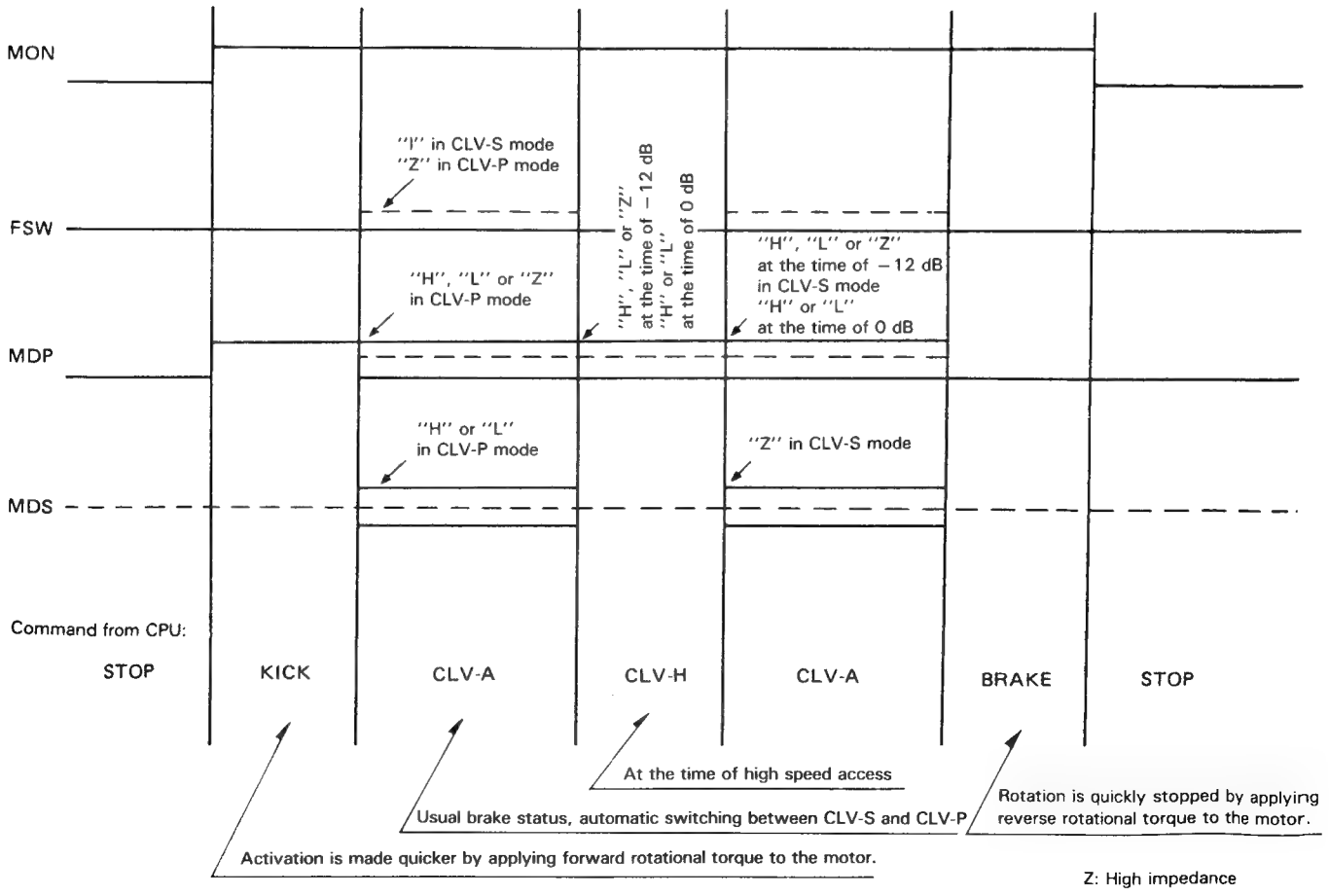


Fig. 9 Typical control of spindle motor

CIRCUIT DESCRIPTION

(4) CLV-S: Register E = 1110'B

Rough servo mode used at the time of start of rotation, at the time of track jump and also when the EFM-PLL circuit is unlocked due to another reason.

When the period of VCO's oscillation frequency 8.6436 MHz is expressed as "T", the pulse width of a frame synchronizing signal is "22T" during specified revolution, and it is the maximum pulse width in a period of RFCK. In practice, however, there are pulses having widths over "22T" due to drop-off of EFM signal due to other reasons, and the frame synchronizing signal cannot be correctly detected unless such pulse are removed. Therefore, the maximum value (peak) of the pulse width of EFM signal is detected (called peak hold) in the period of RFCK/2 or RFCK/4, than the minimum value in this peak is detected (called bottom hold) in the period of RFCK/16 or RFCK/32, and this value is used as the frame synchronizing signal.

"L" is produced out of MDP pin while the frame synchronizing signal is "21T" or less, "Z" when it is "22T", or "H" when it is "23T" or more. Either 0 dB or 12 dB can be selected as its gain.

MDS = "Z", FSW = "L", MON = "H".

(5) CLV-H: Register E = 1100'B

Rough servo mode used at the time of high-speed access.

Assuming there are 20,000 tracks, from the innermost to the outermost, and that this distance is accessed in 1 second, the mirrors (portions where there are no pits) between tracks result in a 20 kHz signal, which is superimposed on the EFM signal. When such a signal is input in the CLV-S mode, a longer mirror section than the actual frame sync signal is detected as the peak value, resulting in an unstable servo.

Therefore, in order to stabilize the servo during high-speed access, the CLV-H mode performs the peak hold at a period of 8.4672/256 MHz (about 34 kHz). Then, like the CLV-S mode, it performs the bottom hold at a period of RFCK/16 or RFCK/32. Except for the period of peak detection, other operations of the CLV-H mode are the same as for the CLV-S mode.

Pwmdx: Pulse width after bottom hold
TB: Bottom hold period, i.e. RFCK/16 or RFCK/32
Z: High impedance

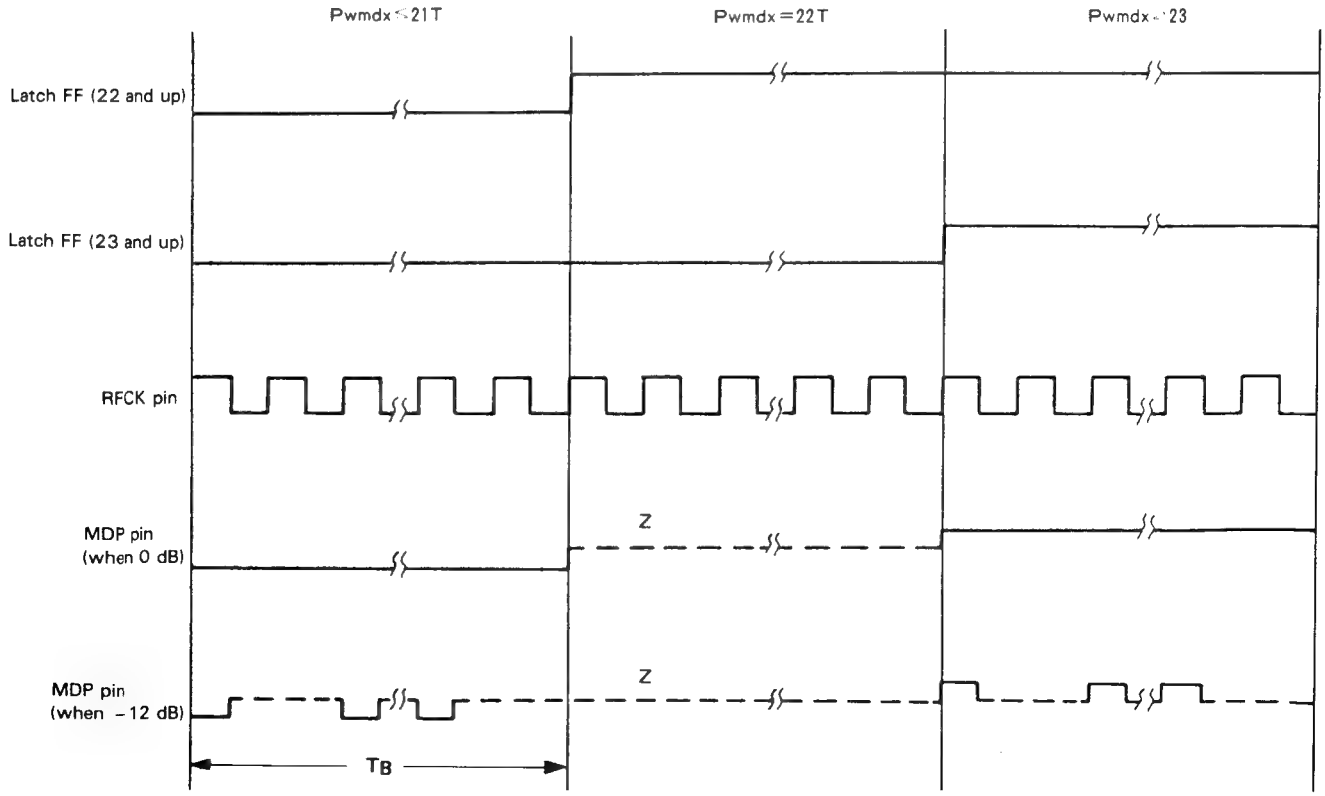


Fig. 10 Timing chart in CLV-S, CLV-H mode (1)

CIRCUIT DESCRIPTION

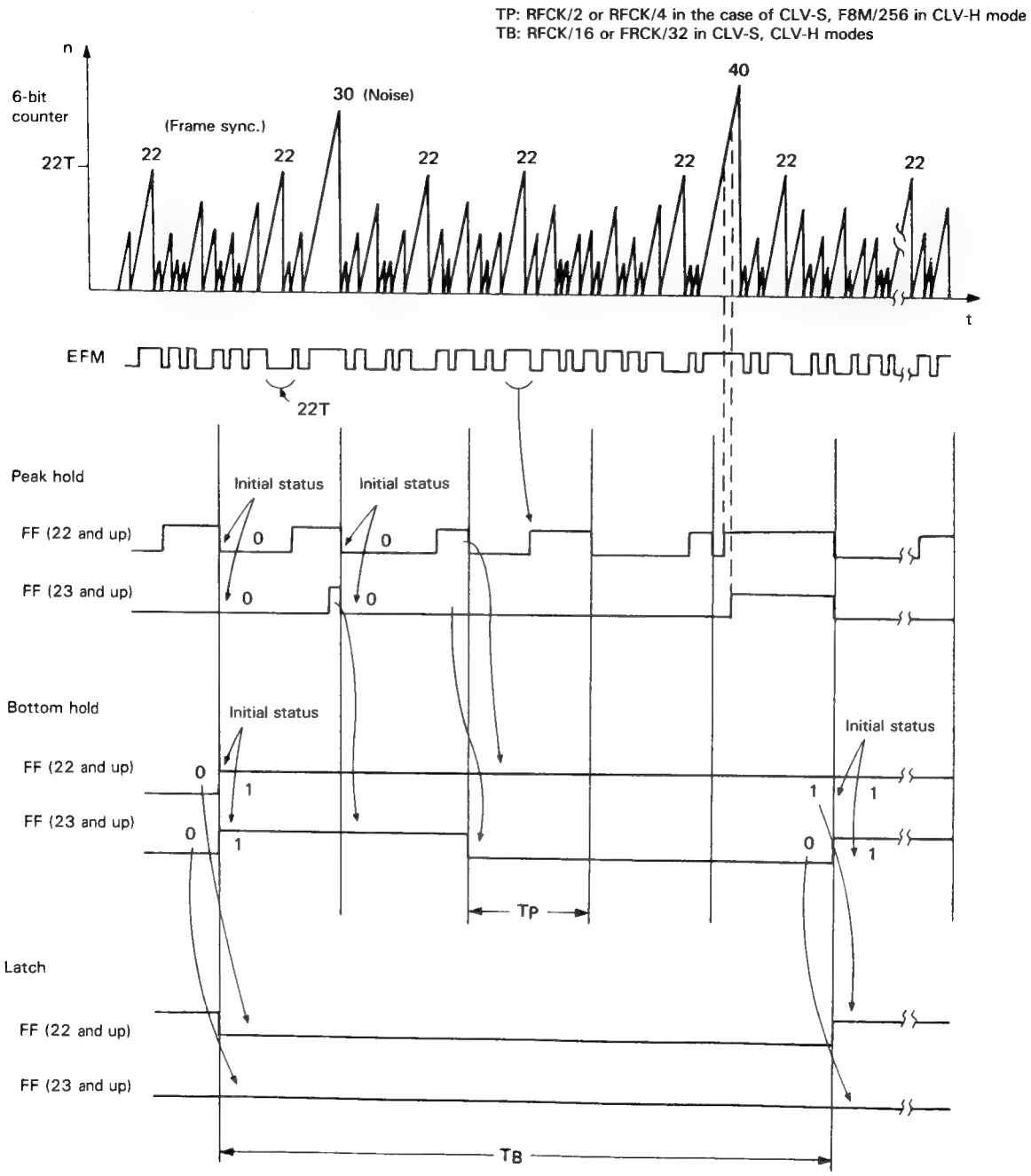
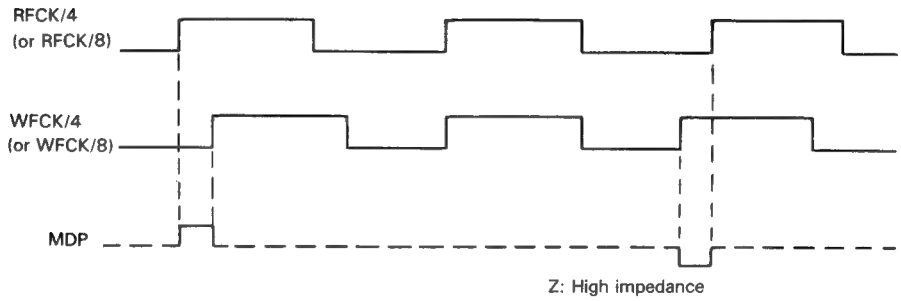


Fig. 11 Timing chart in CLV-S, CLV-H mode (2)

CIRCUIT DESCRIPTION

(6) CLV-P: Register E = 1111'B
PLL servo mode.
When the NCLV of register 9 is "0", the phase of the WFCK/4 signal and the phase of the RFCK/4 signal are compared and output to the MDP pin. When NCLV = "1", 1/4 of the base counter frame frequencies at the Write side and the Read side are phase-compared and output to the MDP pin. It goes "H" when WFCK is slow, "L" when it is fast, and is "Z" when synchronized.
Assuming the 8.4672/2 MHz period is T, and the time when WFCK is "H" is thw, the MDS pin outputs a signal which goes "H" during the time from the trailing edge of WFCK to the time represented by (thw-279T) × 32, and then goes "L" until the next trailing edge of WFCK.
MDS = "H" when thw ≧ 279T,
MDS = "L" when thw ≦ 279T.
The MDS pin varies between 32T and 544T, in 32T steps, when 280T ≦ thw ≦ 296T. For example, when synchronized (rotating at the standard speed), that is when thw = 288T, a 7.35 kHz signal, with a duty cycle of 50% is output.
FSW = "Z", MON = "H".

MDP pin



5) MDS pin (The period of 4.2336 MHz is expressed as "T".)

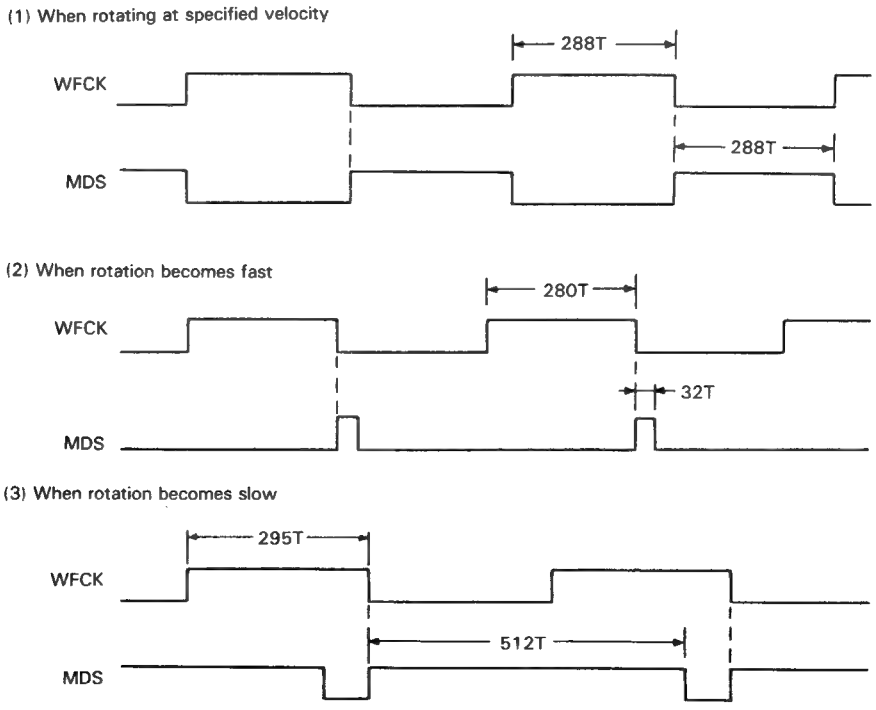


Fig. 12 Timing chart in CLV-P mode

CIRCUIT DESCRIPTION

(7) CLV-A: Register E=0110'B

The mode used for normal play status.

The GFS signal (''H'' when locked, ''L'' when unlocked), after frame sync detection, protection and interpolation block, is sampled at WFCK/16, and functions in CLV-P mode when the signal is ''H''. When the ''L'' signal continues for 8 times, the mode is automatically changed to CLV-S mode.

When in the CLV-S mode, setting of the peak hold period, and setting of the period and gain of the bottom hold of the CLV-S and CLV-H are performed in register D, and the selection of each mode is performed in register E. The description of these registers are detailed in **''1. CPU interface''**. (Page 28)

Note:

When PSSL=''L'', DA07 pin outputs WFCK/4 or WFCK/8 as FCKV, and DA08 outputs EFCK/4 or EFCK/8 as FCKX.

(8) CLV-A': Register E=0101'B

New auto servo mode added to the CX23035.

The difference between CLV-A' and CLV-A is in the rough servo system. With the old rough servo system, the EFM pattern is measured by a crystal and the servo is applied so that the width of the sync pattern is a fixed value, and the rotation speed of the spindle motor is roughly fixed. In this case, if the value is out of the VCO capture range, the VCO never locks with the EFM. With the new rough servo system, a VCO is used for measurement instead of a crystal. If the VCO center is shifted from true center the VCO tends to lock, since the rotation of the spindle motor varies in the same direction.

The new rough servo functions only in CLV-A' mode. The rough servo in CLV-A mode and CLV-S mode is the old rough servo.

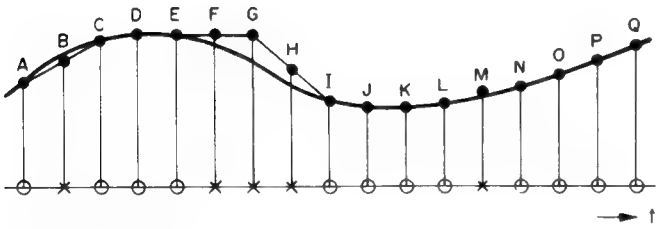
CIRCUIT DESCRIPTION

7. Interpolation and mute, attenuate

(1) Interpolation circuit block

3-byte data can be obtained with a Read to D/A request. They are C2 pointer, less significant 8-bit and motor significant 8-bit. The total 16-bit constitute the data generated per sampling (2's complement.)

The C2 pointer expresses the reliability of this 16-bit data. Therefore, data with C2 pointer is subject to interpolation in this block.



○: Without C2 pointer
X : With C2 pointer

Fig. 13

Mean value interpolation

$$B = \frac{1}{2}(A + C)$$

$$H = \frac{1}{2}(E + I) \qquad \text{: When pointers are continuous}$$

$$M = \frac{1}{2}(L + N)$$

Previous value hold

$$F = G = E$$

16-bit data is alternately output to L-ch and R-ch, R-ch data is output in the section in which LRCK is "L" and L-ch data is output in the section in which LRCK is "H".

C2PO signal outputs C2 pointer to the 16-bit data directed DA01 - DA16 (PSSL = H), DA16 (PSSL = L).

In other words, it means that the 16-bit data that is output when C2PO is "H", is interpolated data.

(2) Explanation of muting and attenuator

In the muting block it is possible to mute ($-\infty$ dB) or attenuate (-12 dB) the audio signal in accordance with the MUTG pin and ATTM signal of the CPU interface block.

When the ZCMT flag of register 9 is "1", the input from the MUTG pin is valid only if all of the audio data higher 6-bit (including the sign bit) are "1" or "0".

Note that switching the MUTG pin does not cause muting if the data zero-cross does not occur. To eliminate this problem, after switching the MUTG pin "H" or "L" with ZCMT = "1", ZCMT shall be turned "0" in a specified period of time, regardless of whether the zero-cross causes muting ON/OFF or not.

ATTM	MUTG	Attenuation value	Remarks
0	0	0 dB	
1	0	−12 dB	
0	1	$-\infty$ dB	(See Note)
1	1	−12 dB	(See Note)

Note:
When the MUTG is set to "H" level with the NCLV flag set to "0", the read base counter value is continuously loaded into the write base counter as well as the muting.
Except at CLV-A, CLV-P, CLV-S, or CLV-A' with the NCLV flag set to "1", the base counter value is loaded.

CIRCUIT DESCRIPTION

8. Mode setting

The various kinds of mode can be set by combining the following pins. (Refer to Table 2.)

MD1 pin : Mainly for selection of the oscillator clock at the XTAI or XTAO pin.
MD2 pin : Mainly for selection of the digital out function.
MD3 pin : Mainly for selection of the digital filter function.
PSSL pin : Mainly for selection between serial and parallel output.
SLOB pin : Selection between offset binary and 2's complement.

Input pin					Function					(Note)	Compatible IC	
MD 1	MD 2	MD 3	PSSL	SLOB	8M/16M	DO OFF/ON	DF OFF/ON	P/S	OB/2's	CD ROM/AUDIO	CXD1125	CXD1130
L	L	L	L	L	16M	DO ON	DF ON	Seri	2's	AUDIO		
L	L	L	H	H	↓	↓	↓	Para	OB	↓		
L	L	H	L	L	↓	↓	DF OFF	Seri	2's	↓	○	
L	H	L	L	L	↓	DO OFF	DF ON	↓	↓	↓		○
L	H	L	H	H	↓	↓	↓	Para	OB	↓		○
L	H	H	L	L	↓	↓	DF OFF	Seri	2's	↓	○	○
L	H	H	H	H	↓	↓	↓	Para	OB	↓	○	○
H	L	L	L	L	8M	↓	DF ON	Seri	2's	↓		○
H	L	L	H	H	↓	↓	↓	Para	OB	↓		○
H	L	H	L	L	↓	↓	DF OFF	Seri	2's	↓	○	○
H	L	H	H	H	↓	↓	↓	Para	OB	↓	○	○
H	H	H	L	L	16M	DO ON	↓	Seri	2's	CD ROM	○	
H	H	H	H	L	8M	DO OFF	↓	↓	↓	↓	○	○

Note:
- **8M/16M: Selection of clock, XTAI or XTAO. 8.4672 MHz/ 16.9344 MHz**
- **DO OFF/ON: Digital out OFF/ON**
- **DF OFF/ON: Digital filter OFF/ON**
- **P/S: Parallel output/serial output**
- **OB/2's: Offset binary/2's complement**
- **CD ROM/AUDIO: Compatible to CD ROM/Compatible to audio**

Table 2

• Selection of clock

The oscillator clock for XTAI and XTAO is available at 16.9344 MHz and 8.4672 MHz. However, when digital output is used, the clock must be set to 16.9344 MHz.

• Selection of digital filter (Refer to "9. Digital filter".)

When the digital filter function is set to ON, the DAC interface signal are all set to double speed.

• Selection of parallel output/serial output

When the parallel output is selected, DA01 to DA16 pins output the 16-bit parallel data.

When the serial output is selected, DA01 to DA16 pin output the following signals respectively.

C1F1 (DA01) :
C1F2 (DA02) : Error correction status monitor output at C1 decode.
C2F1 (DA03) :
C2F2 (DA04) : Error correction status monitor output at C2 decode.

C2FL (DA05) : Correction status output, C2FL = C2F1·C2F2.
C2PO (DA06) : C2 pointer signal.
RFCK (DA07) : Read frame clock signal, 7.35 kHz when locked to the crystal line.
WFCK (DA08) : Write frame clock signal, 7.35 kHz when locked.
$\overline{\text{PLCK}}$ (DA09) : 1/2 of the divided signal from the VCO pin, 4.3218 MHz when locked.
UGFS (DA10) : Non-protected frame sync signal.
GTOP (DA11) : Frame sync protect status display signal.
RAOV (DA12) : Jitter margin over or underflow display signal.
C4LR (DA13) : 4 times the LRCK signal.
$\overline{\text{C21O}}$ (DA14) : Bit clock (invert signal of C21O).
C21O (DA15) : Internal system clock (2.1168 MHz).
DATA (DA16) : Serial data output (MSB or LSB first output).

CIRCUIT DESCRIPTION

• Selection of offset binary/2's complement

When the SLOB pin is "H", an offset binary signal is output, and when it is "L", a 2's complement signal is output.

• Selection of CD ROM/audio compatibility

When MD1 = MD3 = "H", the player is compatible with a CD ROM and outputs the C2 pointer for each byte. At the same time, the average value interpolation and the previous value holding operations are not performed. For example, when there is an error in the upper 8-bit of the 16-bit, only the C2 pointer corresponding to the upper 8-bit goes "H", and the lower 8-bit are processed as the correct data.

9. Digital filter

The built-in digital filter has the following features:

1. Correction of the aperture effect
2. Small attenuation at 20 kHz
3. Practical-design filtering band ranges

(1) Filter characteristics

Passing Band	Ripple from DC to 18 kHz	±0.07 dB max.
	Attenuation of 20 kHz with respect to 1 kHz	0.65 dB max.
Filtering Band	Attenuation of 44.1 ± 1 kHz with respect to 1 kHz	87 dB min.
	Attenuation of 44.1 ± 5 kHz with respect to 1 kHz	58 dB min.
	Attenuation of 44.1 ± 10 kHz with respect to 1 kHz	44 dB min.
	Attenuation of 44.1 ± 20 kHz with respect to 1 kHz	10 dB min.
	Frequency range in which attenuation is −30 dB with respect to 1 kHz	44.1 ± 14 kHz
	Frequency range in which attenuation is −60 dB with respect to 1 kHz	44.1 ± 4 kHz

10. Countermeasures to defect

To counter a defect, the PDO pin is set to "Hi-Z" during the time until GFS goes "H" again after inverting from "H" to "L" or after about 0.55 ms has elapsed. However, this operation is performed only when the HZPD flag of register 9 is "1". When HZPD = "0", it will never be set to "Hi-Z".

The signal switching between the rough servo in the CLV-A or CLV-A' mode and the PLL servo is output from the LOCK Pin.

After the GFS signal is sampled at WFCK/16, and when the signal is "1", the LOCK pin goes "H", when a "0" is present 8 times in a row, the LOCK pin goes "L".

This operation is similar to that for the FSW pin.

However, while the FSW outputs a fixed signal when not in CLV-A or CLV-A' mode, the LOCK pin always output the above signal.

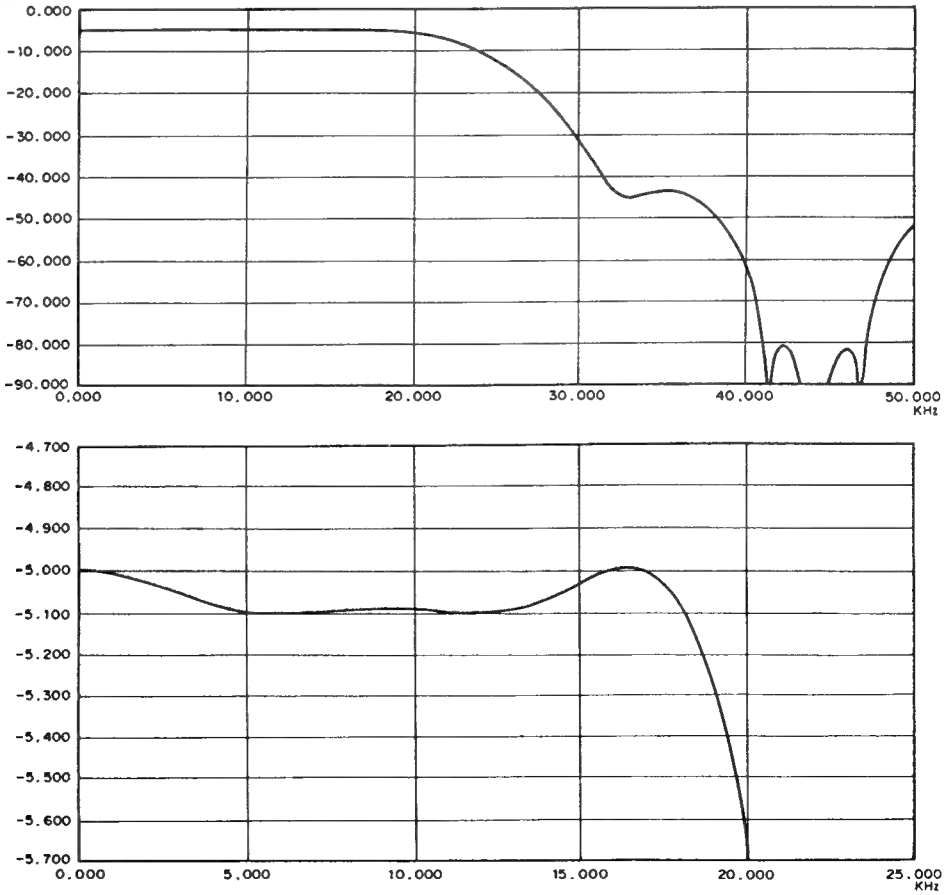
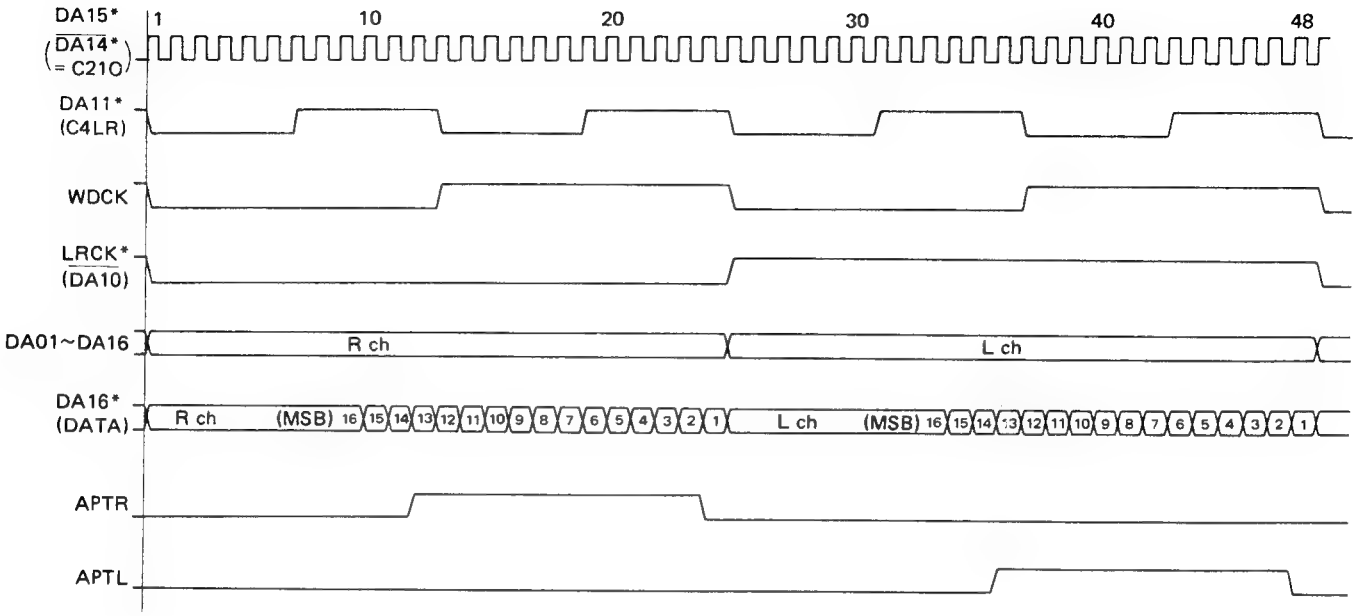


Fig. 14 Frequency characteristic after sample & hold

CIRCUIT DESCRIPTION

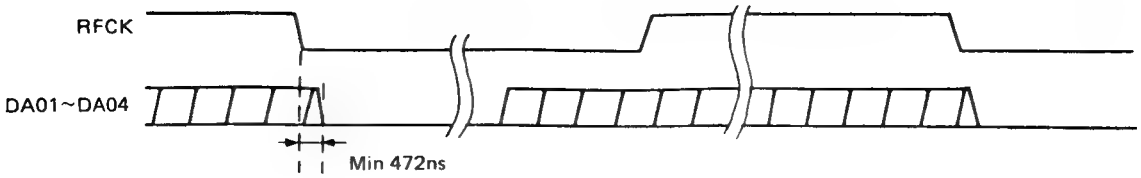
- **Timing chart**



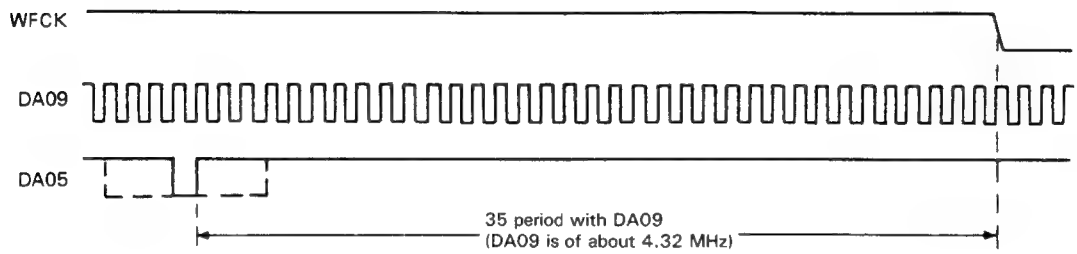
* When PSSL = "L".

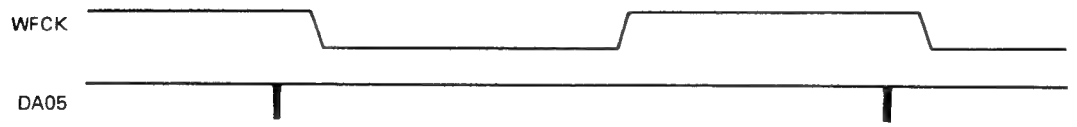
Fig. 15 Timing chart of audio output

CIRCUIT DESCRIPTION



* DA01 to DA04 (C1F1, C1F2, C2F1, C2F2) are cleared when a period of minimum 472 ns has elapsed since RFCK was deactivated.
* AND signal of C2F1 and C2F2 is output out of C2FL pin.





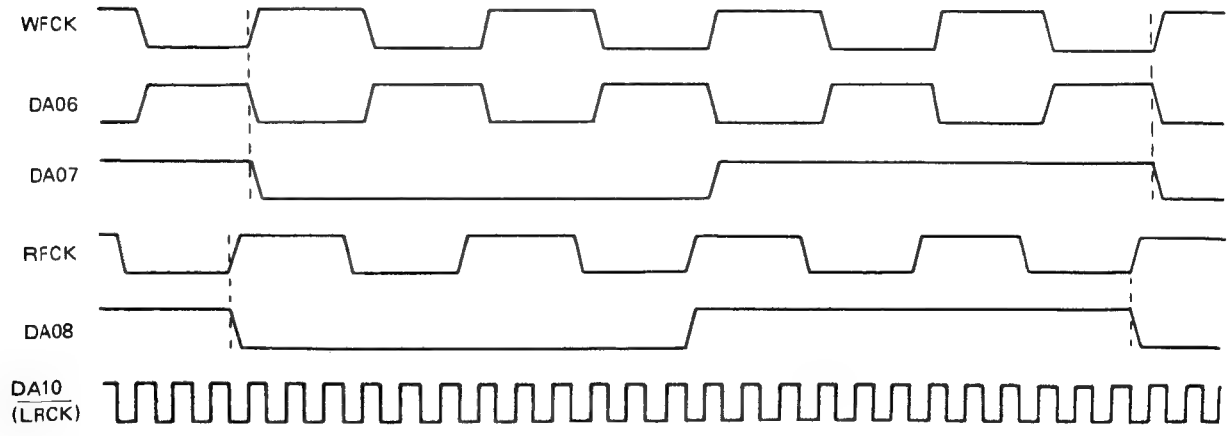


Fig. 16 Timing chart of DA01 to DA16 output when PSSL = "L"

CIRCUIT DESCRIPTION

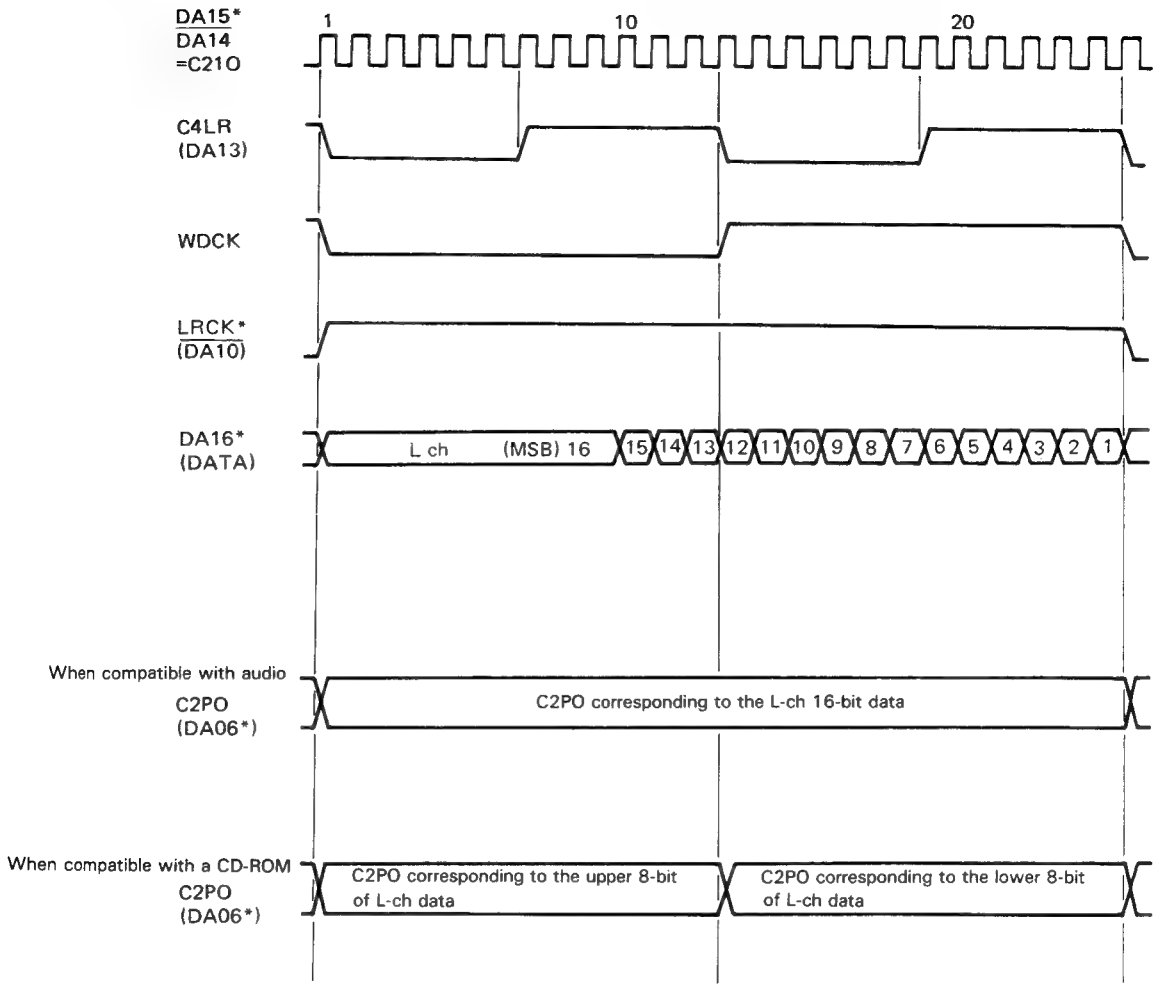


Fig. 17 Timing chart of C2PO output (when PSSL = "L")

* RAOV becomes "H" for one frame (synchronized with WFCK) when a jitter that exceeds ±4 frames is generated between RFCK and WFCK.

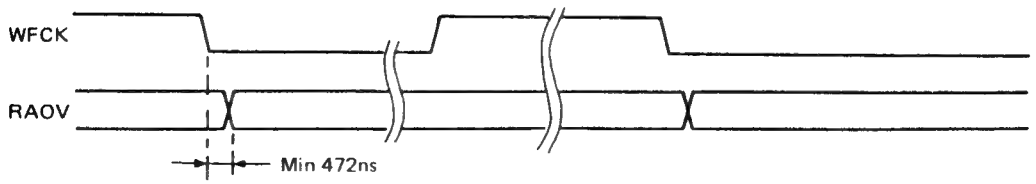


Fig. 18 Timing chart of RA0V output

CIRCUIT DESCRIPTION

U403: CMOS 4-BIT, 1-CHIP MICROPROCESSOR (CXP5024H)

General

The CXP5024H is a CMOS 4-bit microprocessor, which incorporates a 4-bit CPU, ROM, RAM, I/O ports, an 8-bit timer, an 8-bit timer/counter, an 18-bit time base timer, an 8-bit serial I/O, a vector interrupt function and a power-on reset function, as well as an LCD controller/driver and a standby function for low power consumption, in a single chip.

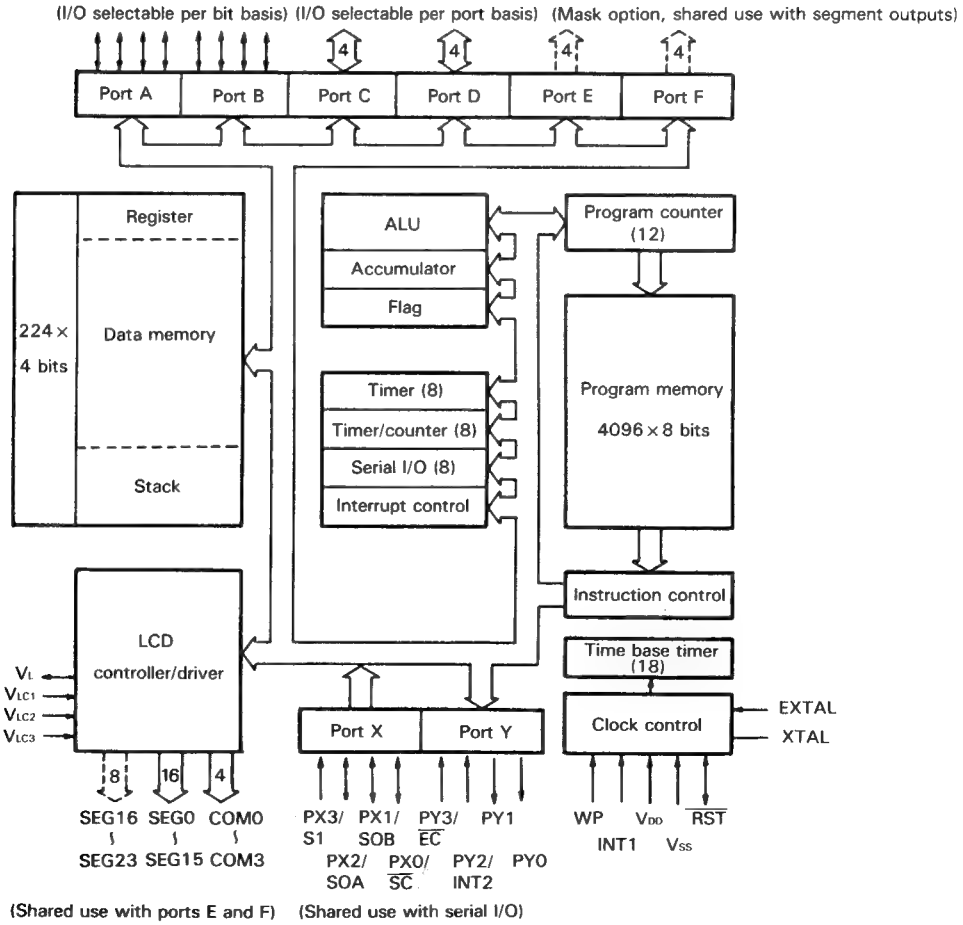
Features

- Basic instruction cycle: 3.8 μs/4.19 MHz, 1.9 μs/4.19 MHz (High-speed version)
- ROM capacity: 4,096×8 bits
- RAM capacity: 224×4 bits (24×4 bits of which are also used as an LCD display memory)
- General-purpose I/O ports with 32 lines (16 of which are used for segment output)
- LCD controller/driver with direct-drive capability. The segment output lines can optionally be selected to 24, 20 or 16. The duty cycle is programmable to 1/3 or 1/4. 1/3 bias.
- Two external interrupt terminals.
- 8/4-bit variable serial I/O.
- Independently-controllable 8-bit timer, 8-bit timer/event counter and 16-bit time base timer.
- Arithmetic and logic operations between all RAM and I/O areas, and an accumulator using memory-mapped I/O.
- Reference to all ROM area using table look-up instructions.
- Two power-down modes: Sleep, Stop.
- Power-on reset circuit.
- Either crystal or CR oscillator can be selected optionally.

Structure

Silicon gate CMOS IC

Block diagram



CIRCUIT DESCRIPTION

Terminal explanations

Terminal No.	Terminal name	I/O	Signal name	Active H/L	Function
1	PY0	O	POWER ON/OFF	H OFF L ON	POWER ON/OFF signal.
2	PY1	O	MUTG	H ON L OFF	Muting output. In normal operation, MUTG is "L" when internal register ATTM is "L".
3	INT2/PY2	I	LIMIT SW	H OUT L IN	Innermost limit switch input.
4	$\overline{EC}$/PY3	O	SENCE		Internal status output according to address.
5	$\overline{SC}$/PX0	O	SQCK	⎍	Sub code Q read clock.
6	SOB/PX1		SOB/PX1		GND (0 V)
7	SOA/PX2		SOA/PX2		GND (0 V)
8	SI/PX3	I	SUBQ		Sub code Q input.
9	PD0	O	EMPHA	H ON L OFF	Disc emphasis ON/OFF signal.
10	PD1	O	LASER	L ON H OFF	Laser ON/OFF signal.
11	PD2	O	HIFILTER	H ON L OFF	Hi-Filter ON/OFF signal.
12	PD3				
13	PC0	I	KIN3		MSB Key latch input port. LSB
14	PC1	I	KIN2		
15	PC2	I	KIN1		
16	PC3	I	KIN0		
17	PB0	I	FOK	H OK L NG	Focus OK signal.
18	PB1	I	ATSC	H ON L OFF	ATSC ON/OFF signal.
19	PB2	I	OPEN/CLOSE	H OPEN L CLOSE	Open/Close signal.
20	PB3	I	LOW BATT	H L LOW	Battery voltage alarm signal.
21	PA0	I	TEST TP	H NORMAL L TEST	Microprocessor test mode activation terminal. (0 V)
22	PA1	O	KS1	L LATCH	Key latch output port.
23	PA2	O	KS2		
24	PA3	O	KS3		
25	V_{SS}		V_{SS}		GND. (0V)
26	V_{DD}		V_{DD}		Power supply. (+5 V)
27	PE3 SEG23	O	$\overline{XRST}$	L	System reset output.
28	PE2 SEG22	O	DATA		Serial data output from the CPU.
29	PE1 SEG21	O	XLT	⎍	Latch output from the CPU.

CIRCUIT DESCRIPTION

Terminal No.	Terminal name	I/O	Signal name	Active H/L	Function
30	SEG20 PE0	O	CLK		Clock output for serial data transfer from the CPU.
31	SEG19 PF3	O	SEG19		Display segment outputs.
32	SEG18 PF2	O	SEG18		
33	SEG17 PF1	O	SEG17		
34	SEG16 PF0	O	SEG16		
35	SEG15	O	SEG15		
36	SEG14	O	SEG14		
37	SEG13	O	SEG13		
38	SEG12	O	SEG12		
39	SEG11	O	SEG11		
40	SEG10	O	SEG10		
41	SEG9	O	SEG9		
42	SEG8	O	SEG8		
43	SEG7	O	SEG7		
44	SEG6	O	SEG6		
45	SEG5	O	SEG5		
46	SEG4	O	SEG4		
47	SEG3	O	SEG3		
48	SEG2	O	SEG2		
49	SEG1	O	SEG1		
50	SEG0	O	SEG0		
51	COM3				Common display segment outputs.
52	COM2	O	COM2		
53	COM1	O	COM1		
54	COM0	O	COM0		
55	VLC1		VLC1		
56	VLC2		VLC2		
57	VLC3		VLC3		
58	V_{DD}		V_{DD}		Power supply. (+5 V)

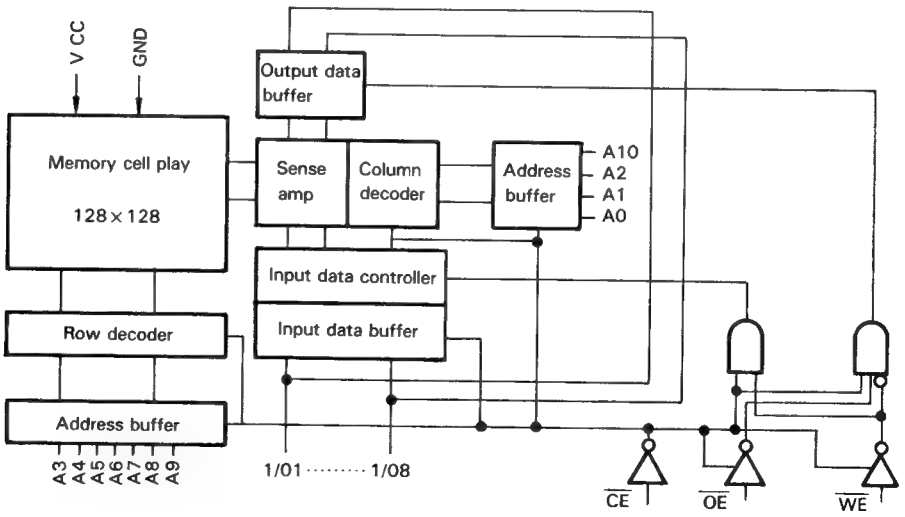
CIRCUIT DESCRIPTION

Terminal No.	Terminal name	I/O	Signal name	Active H/L	Function
59	VL	O	VL		
60	XTAL	O	XTAL		CR oscillator output. (f=4.19 MHz)
61	EXTAL	I	EXTAL		
62	$\overline{RST}$	I	RESET	L	Microprocessor reset input.
63	WP				
64	INT1	O	SCOR	⎍↑	Sub code sync S0+S1 output.

U402: STATIC RAM (LC3517ALM-15)

Function
2048-word×8-bit static RAM
Application
Memory system, battery-driven portable system

Block diagram



CIRCUIT DESCRIPTION

U404: Digital filter for CD players (SM5807ES)

General

The SM5807ES is a quadruple-oversampling digital filter for CD players, developed using molybdenum-gate CMOS technology. This LSI incorporates digital filters for both channels and outputs quadruple-oversampling signals for both channels, thereby making it possible to simplify the analog filters in subsequent stages.

Features

- TTL-compatible inputs/outputs.
- Single power supply of 5 V±0.5 V.
- Serial inputs/outputs that allow the production of a compact system.

Functions

- Quadruple oversampling.
- 2-channel filtering.
- Built-in overflow limiter.
- 16-bit serial input/output (2's complement, MSB first).
- Built-in X'tal oscillator circuit.
- XT terminal input clock buffer output.

Structure

- 16-pin plastic SOP.

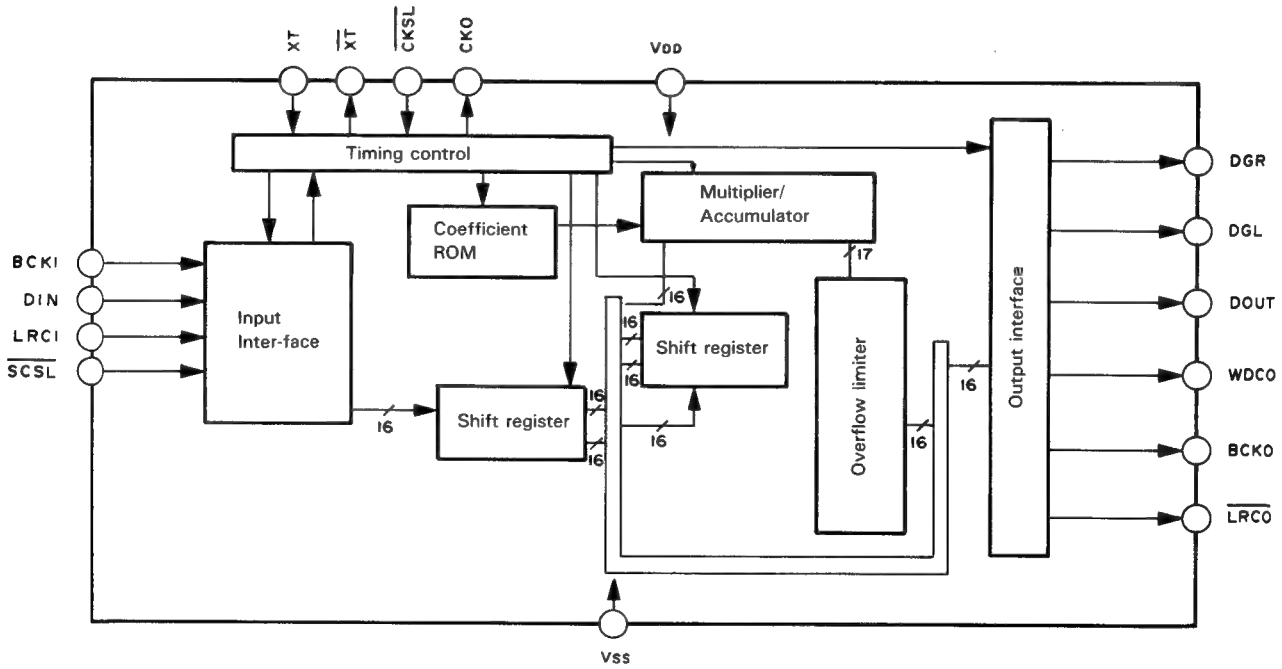
Filter configuration

- Linear-phase FIR filter, in a 2-stage successive connection (61-order + 13-order).

Filter Characteristics

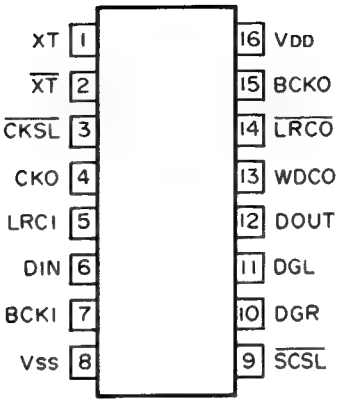
- Pass band and ripple 0 to 20 kHz: 0.05 dB or less
- Stopping band and attenuation 24.1 kHz or more: 45 dB or more
- Linear phase (No group delay distortion).

Block Diagram



CIRCUIT DESCRIPTION

Pin configuration



Terminal explanations

Note) I : Input terminal (Ip incorporates a pull-up resistor.)
O : Output terminal

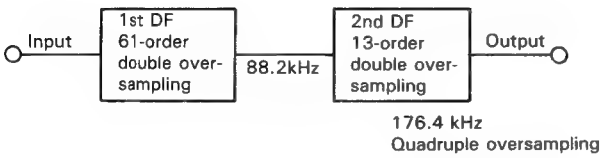
Terminal No.	Terminal name	I/O	Function
1	XT	I	Oscillator input terminal.
2	XT	O	Oscillator output terminal.
3	CKSL	Ip	H: X'tal oscillator signal, or external clock of 16.9344 MHz or 17.2872 MHz, is input to XT. L: X'tal oscillator signal, or external clock of 8.4672 MHz or 8.6436 MHz, is input to XT.
4	CKO	O	Clock output.
5	LRCI	Ip	44.1 kHz sync clock input.
6	DIN	Ip	Serial data input.
7	BCKI	Ip	Serial input bit clock input.
8	Vss	—	GND terminal (0 V).
9	$\overline{\text{SCSL}}$	Ip	H: System clock = 192 fs (fs: Sampling frequency). L: System clock = 196 fs.
10	DGR	O	R CH deglitch signal (176.4 kHz).
11	DGL	O	L CH deglitch signal (176.4 kHz).
12	DOUT	O	Serial data output.
13	WDCO	O	Output control clock (352.8 kHz).
14	$\overline{\text{LRCO}}$	O	Output control clock (176.4 kHz).
15	BCKO	O	Serial output bit clock (8.4672 MHz or 8.6436 MHz).
16	Vdd	—	Power supply terminal (5 V).

CIRCUIT DESCRIPTION

Quadruple Oversampling

This LSI incorporates digital filter circuitry for 2 channels, providing quadruple oversampling outputs for both channels. The SM5807 consists of two linear-phase FIR filters, each of which performs double oversampling, connected in two successive stages.

The basic configuration is shown in the diagram below. Namely, the input signal sampled at 44.1 kHz is first converted by the 61-order 1st DF, with double oversampling, into a signal sampled at 88.2 kHz. The 13-oder 2nd DF converts the input signal with an 88.2 kHz sampling rate, again by double oversampling, and outputs a signal with an 176.4 kHz sampling rate, which is 4 times oversampled when compared to the 1st DF input.



System Clock

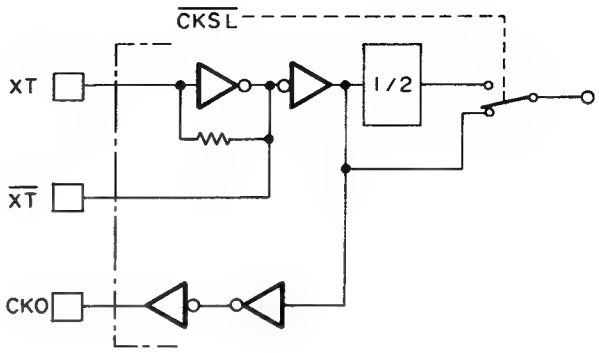
The system clock of the LSI is 192 fs = 8.4672 MHz or 196 fs = 8.6436 MHz.

Either frequency can be selected by the status of the $\overline{SCSL}$ pin.

$\overline{SCSL}$ = H (or Open) ....192 fs (compatible with a 96 fs system clock)

$\overline{SCSL}$ = L.....196 fs (compatible with a 98 fs system clock)

Clock Generator Circuit



Serial Input (data and bit clock)

As the serial input data is input at the positive-going edge of the serial input bit clock BCK1, the data should be valid by the positive-going edge of BCK1. After the 16-bit serial data input, the serial data is latched by the internal register based on the sync clock LRCI. The data should be input in 2's complement format, with the MSB first.

Start of Operations

All operations are started at the positive-going edge of the sync clock LRCI.

Serial output (data and bit clock)

As DOUT outputs the L-CH and R-CH serial data alternately, the output can be converted using only one DAC. In-phase conversion using two DACs is also available by using some external circuitry (2 gates). The data is output in 2's complement format, with the MSB first.

The serial output bit clock is output from the BCKO terminal. As the data varies in synchronism with the positive-going edge of the bit clock, it can be input to the DAC at the negative-going edge.

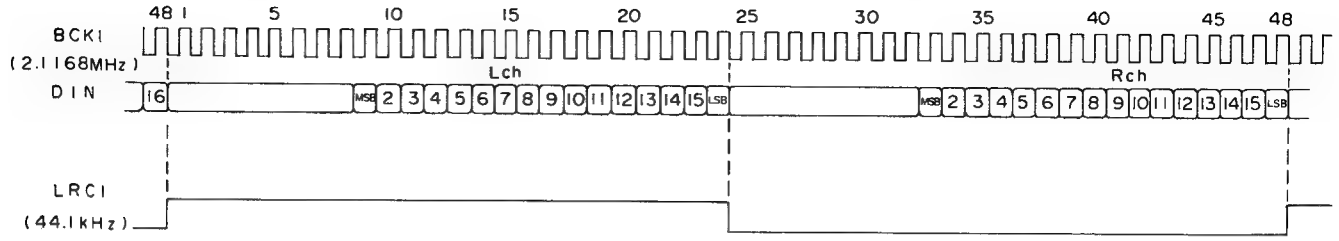
BCKO = 8.4072 MHz
(when SCLS = H or Open, system clock = 192 fs)
BCKO = 8.6436 MHz
(when SCSL = L, system clock = 196 fs)

Deglitch Signal

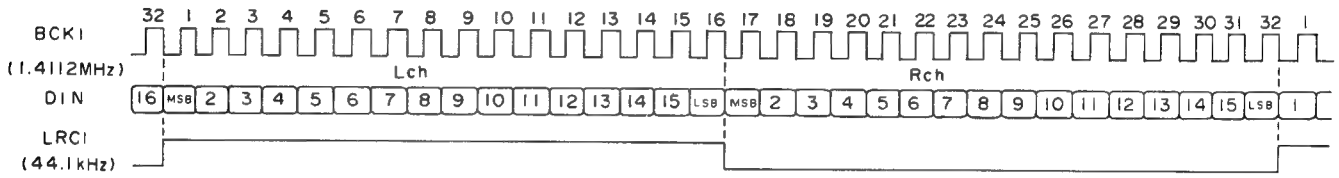
DGL: L CH deglitch signal, 176.4 kHz (25% duty)
DGR: R CH deglitch signal, 176.4 kHz (25% duty)

CIRCUIT DESCRIPTION

Timing chart

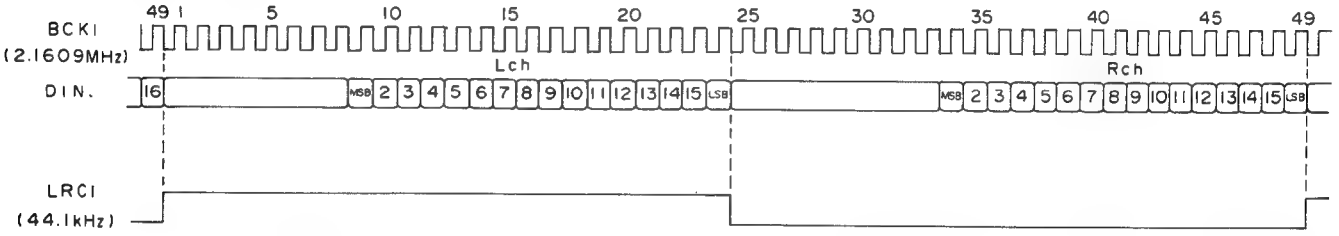


(a)

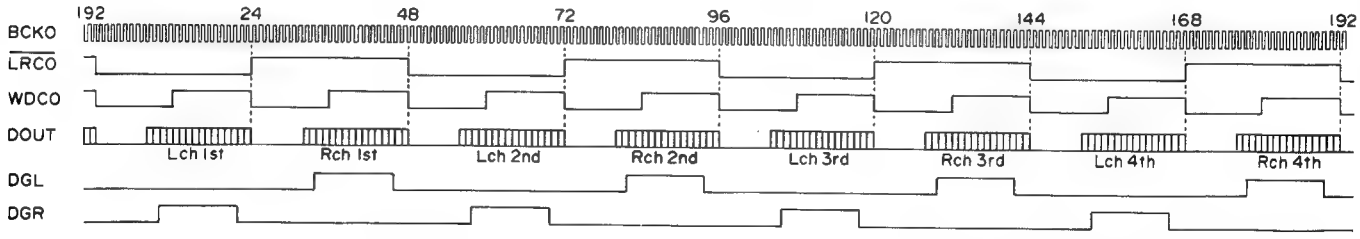


(b)

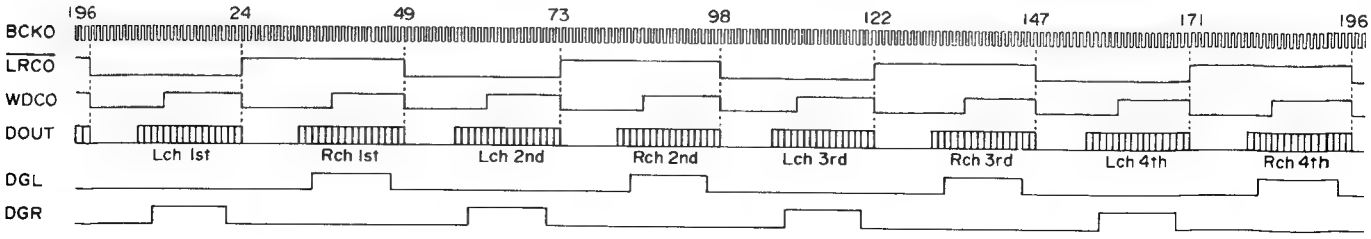
When serial input timing $\overline{SCSL}$ = H (or Open)



When serial input timing $\overline{SCSL}$ = L



When serial input timing $\overline{SCSL}$ = H (or Open)



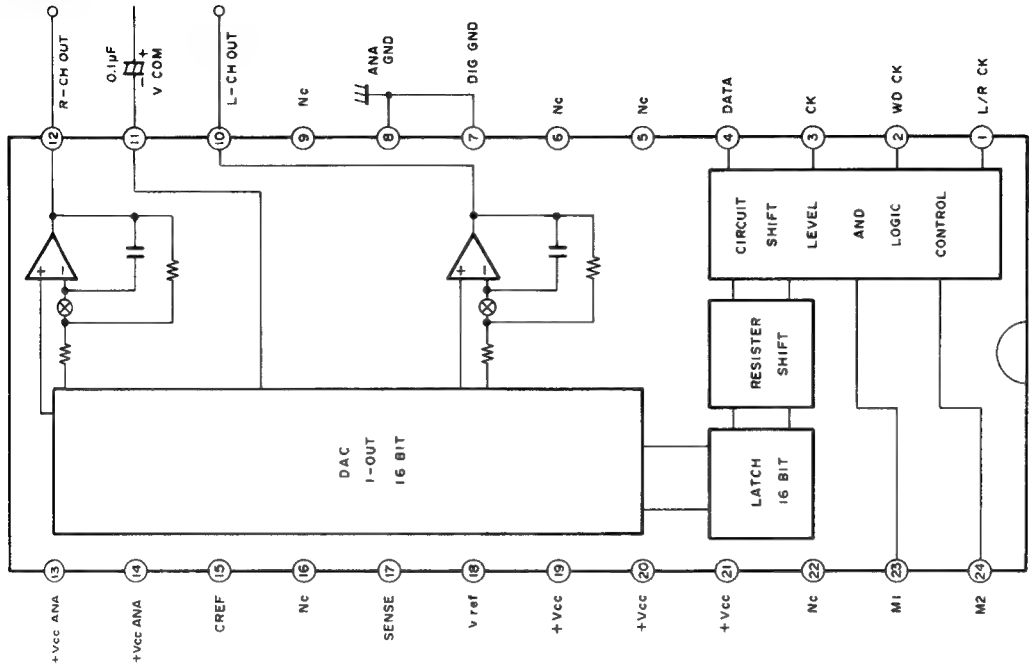
When serial input timing $\overline{SCSL}$ = L

Note: When SCSL = L, the output WDCO cycle is not constant. However, DGL and DGR are constant at 176.4 kHz (duty 25%).

CIRCUIT DESCRIPTION

U501: 16-bit D/A CONVERTER (PCM60P-KY)

Block diagram



Terminal explanations

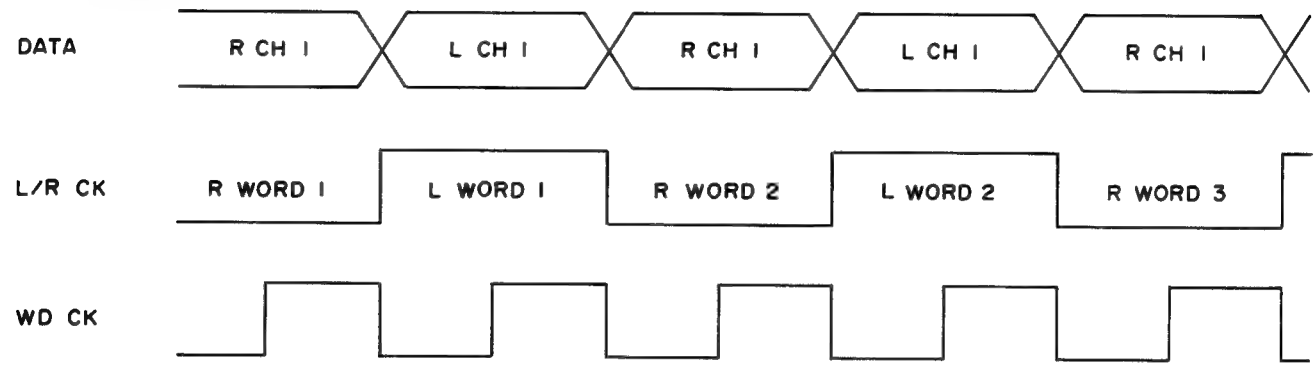
Terminal No.	Terminal name	Function
1	L/R CK	LR clock input terminal.
2	WD CK	Word clock input terminal.
3	CK	Clock input terminal.
4	DATA	Digital audio data input terminal.
5	NC	No connection.
6	NC	No connection.
7	DIG GND	Digital GND terminal.
8	ANA GND	Analog GND terminal.
9	NC	No connection.
10	L-ch OUT	L-ch output terminal.
11	V COM	V common terminal.
12	R-ch OUT	R-ch output terminal.
13	+Vcc	Supply voltage terminal.
14	+Vcc	Supply voltage terminal.
15	C REF	Reference capacity connection terminal.
16	NC	No connection.
17	Vref Sense	Reference sensitivity setting terminal.
18	Vref	Reference voltage input terminal.
19	+Vcc	Supply voltage terminal.
20	+Vcc	Supply voltage terminal.
21	+Vcc	Supply voltage terminal.
22	NC	No connection.
23	M1	Mode 1 input terminal.
24	M2	Mode 2 input terminal.

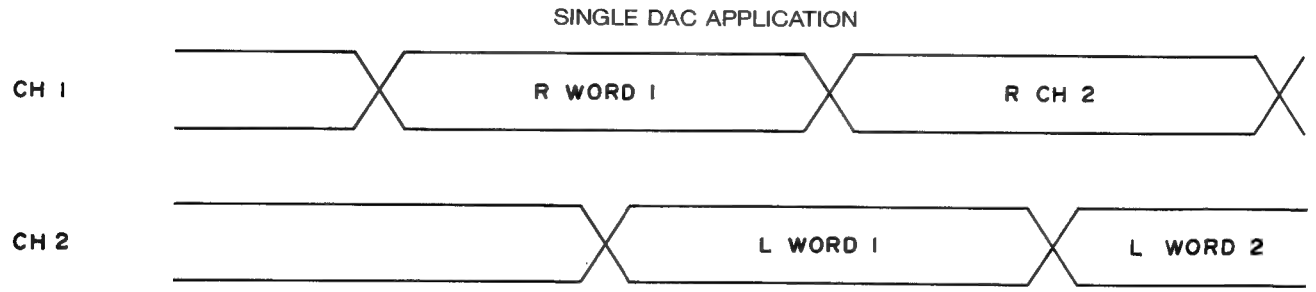
CIRCUIT DESCRIPTION

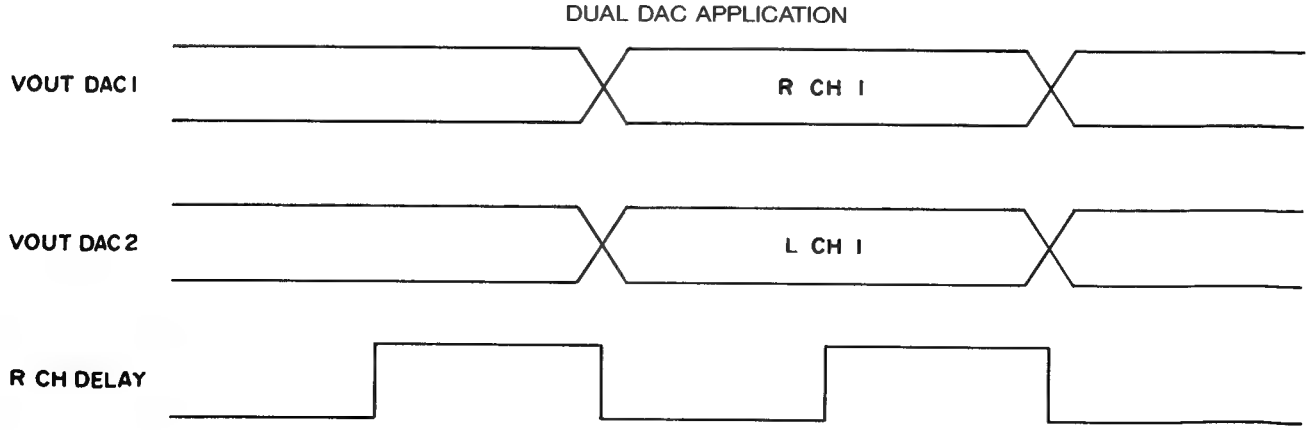
Function mode

MODE 1	MODE 2	
PIN23	PIN24	FUNCTION
0	0	STEREO
0	1	STEREO (NO DIFFERENCE)
1	0	LEFT CHANNEL ONLY (FROM RIGHT.RO)
1	1	RIGHT CHANNEL ONLY

Timing diagram







Fs 44.1kHz 88.1kHz
2Fs 88.2kHz 176.4kHz

ADJUSTMENT/REGLAGES

ADJUSTMENT

Order	Item	Input Setting	Output Setting	Player Setting	Adjustment Point	Adjustment Method	Fig.
Remove the cover (bottom case).							
1	D/D converter	—	Connect a DC voltmeter to the Vdd terminal.	PLAY	RV1	4.6+0.05/−0 V (Adjust by setting the supply voltage to 5.0 V.)	(a)
2	PLL	—	Connect the ASY terminal to GND, and connect a frequency counter to the PLL terminal.	STOP	RV301	4.26±0.01 MHz	(b)
Caution: After the PLL adjustment, be sure to remove the wire connecting the ASY terminal to GND.							
3	Focus offset	Test disc (Type 4)	Connect an oscilloscope to the EYE terminal.	PLAY	RV102	Adjust for an optimum eye pattern.	(c)
4	Vary the method of placing the set, and make sure that the eye pattern does not vary considerably.						(c)
5	Tracking balance	Test disc (Type 4)	Connect an oscilloscope across the TE and VC terminals.	Play the disc, enter Test mode, then press the REPEAT key. (Connect the TEST terminal to GND.)	RV101	Adjust so that the waveform is symmetrical above and below 1/2 Vcc. DC=0±10 mV	(d)
6	Tracking gain	Test disc (Type 4)	Connect an AC voltmeter to the T.OUT terminal via a 1 kHz BPF, and connect AG (1 kHz, 0.2 V) to the T.IN terminal.	PLAY	RV302	Adjust for maximum reading.	(e)
7	DAC OUT level	Test disc (Type 4)	Connect an oscilloscope to the DAC OUT terminal.	PLAY	RV501	2.5±0.05 Vp-p (1 kHz)	(f)

*When checking a PC board by extending it, use the connector cord (extension cord) used with the DPC-7.

REGLAGES

Ordre	Atricle	Réglage d'entrée	Réglage de sortie	Réglage de lecteur	Point d'ajustement	Méthode d'ajustement	Figure
Retirer le couvercle (coffret du dessous).							
1	Convertisseur N/N	—	Raccorder un voltmètre CC à la borne Vdd.	PLAY	RV1	4,6+0,05/−0 V (ajuster en réglant l'alimentation sur 5,0 V.)	(a)
2	PLL	—	Raccorder la borne ASY à GND et raccorder un compteur de fréquence à la borne PLL.	STOP	RV301	4.26±0.01 MHz	(b)
Attention: Après le réglage PLL, bien retirer le fil connectant la borne ASY à GND.							
3	Décalage de mise au point	Disque test (type 4)	Raccorder un oscilloscope à la borne EYE.	PLAY	RV102	Ajuster pour une forme oculaire optima.	(c)
4	Varier la méthode de placement de l'appareil et s'assurer que la forme oculaire ne varie pas trop.						(c)
5	Balance de l'alignement	Disque test (type 4)	Raccorder un oscilloscope entre les bornes TE et VC.	Lire le disque, entrer en mode de test puis presser la touche REPEAT. (Raccorder la borne TEST à GND.)	RV101	Ajuster pour que la forme d'onde soit symétrique au dessus et en dessous de 1/2 Vcc. CC=0±10 mV	(d)
6	Gain d'alignement	Disque test (type 4)	Raccorder un voltmètre CA à la borne T.OUT via 1 FPB 1 kHz et connecter AG (1 kHz, 0,2 V) à la borne T.IN.	PLAY	RV302	Ajuster pour une lecture maxima.	(e)
7	Niveau de sortie DAC	Disque test (type 4)	Raccorder un oscilloscope à la borne DAC OUT.	PLAY	RV501	2,5±0,05 Vp-p (1 kHz)	(f)

*Lors de la vérification d'une plaquette CI en l'étendant, utiliser un câble connecteur (câble de prolongement) employé avec le DPC-7.

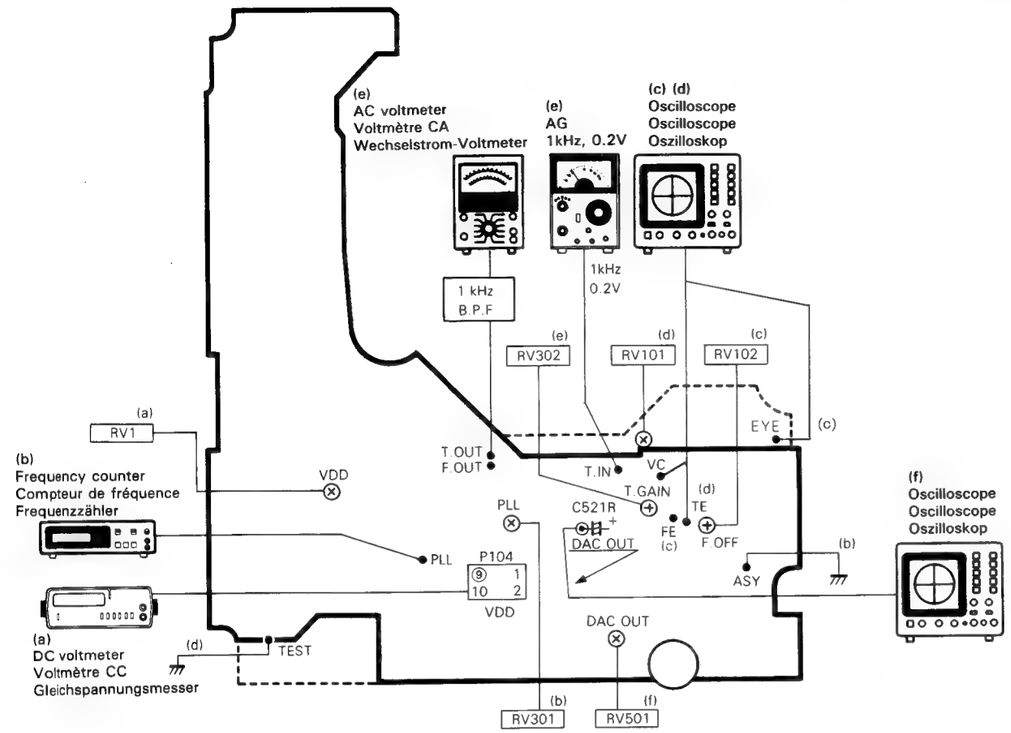
ABGLEICH

ABGLEICH

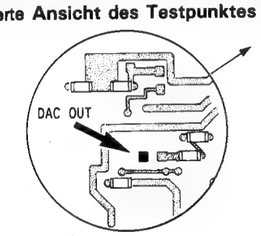
Reihenfolge	Gegenstand	Eingangs-Einstellung	Ausgangs-Einstellung	Spieler-Einstellung	Einstellpunkt	Einstellmethode	Abb.
Die Abdeckung (Bodengehäuse) entfernen.							
1	D/D-Konverter	—	Ein Gleichstrom-Voltmeter an die Klemme Vdd anschließen.	PLAY	RV1	4,6 + 0,05/ − 0 V (Durch Einstellung der Zuführspannung auf 5,0 V einstellen.)	(a)
2	PLL	—	Die Klemme ASY mit GND verbinden und einen Frequenzzähler an die Klemme PLL anschließen.	STOP	RV301	4.26 ± 0.01 MHz	(b)
Zur Beachtung: Nach der PLL-Einstellung unbedingt den Draht zwischen der Klemme ASY und GND entfernen.							
3	Fokusversatz	Testdisc (Typ 4)	Ein Oszilloskop an die Klemme EYE anschließen.	PLAY	RV102	Auf das optimale Augenmuster einstellen.	(c)
4	Das Gerät anders aufstellen und sicherstellen, daß das Augenmuster sich nicht stark verändert.						(c)
5	Spurhalte-Balance	Testdisc (Typ 4)	Ein Oszilloskop an die Klemmen TE und VC anschließen.	Die Disc wiedergeben, den Testmodus aktivieren und die REPEAT-Taste drücken. (Die Klemme TEST mit GND verbinden.)	RV101	So einstellen, daß die Wellenform oberhalb und unterhalb von 1/2 Vcc symmetrisch ist. Gleichstrom = 0 ± 10 mV	(d)
6	Spurhalte-Verstärkung	Testdisc (Typ 4)	Einen Wechselstrom-Voltmeter über einen 1 kHz Bandpaßfilter an die Klemme T.OUT anschließen und AG (1 kHz, 0,2 V) mit der Klemme T.IN verbinden.	PLAY	RV302	Auf die maximale Anzeige einstellen.	(e)
7	DAC OUT Pegel	Testdisc (Typ 4)	Ein Oszilloskop an die Klemme DAC OUT anschließen.	PLAY	RV501	2,5 ± 0,05 Vp-p (1 kHz)	(f)

*Wenn eine Platine zum Überprüfen herausgezogen wird, das Verbindungskabel (Verlängerungskabel), das mit dem DPC-7 verwendet wird, verwenden.

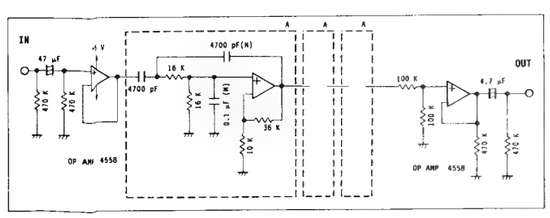
ADJUSTMENT/REGLAGES/ABGLEICH



Magnified View of the DAC OUT Test Point
Vue agrandie du point de test DAC OUT
Vergrößerte Ansicht des Testpunktes DAC OUT



Circuit Diagram of a 1 kHz Band-Pass Filter
Diagramme des circuits d'un filtre passe-bande de 1 kHz
Schaltplan eines 1 kHz Bandpaßfilters



- Test points T.OUT, F.OUT, PLL, FE, TE and ASY are found on the lower PC board.
- For the measurements, use a test rod with a thin tip and insert it through the holes in the upper PC board.

- Les points test T.OUT, F.OUT, PLL, FE, TE et ASY se trouvent sur la plaquette de circuits imprimés inférieure.
- Pour les mesures, utiliser une tige test avec une fine extrémité et l'insérer dans les trous dans la plaquette de circuits imprimés supérieure.

- Die Testpunkte T.OUT, F.OUT, PLL, FE, TE and ASY befinden sich auf der unteren Platine.
- Für die Messungen einen Prüfstift mit einer dünnen Spitze verwenden und diesen durch die Öffnungen in der oberen Platine einführen.

TROUBLESHOOTING

EXPLANATION OF OPERATIONS

1. Supply power to the set from an AC adapter or rechargeable battery.

2. Switch the POWER ON.

3. a) When the lid is open, the display is: 0 (1 digit of the track No.)
b) When the lid is closed, the display is: 00'00"00 (flashing)

4. Operation of the mechanism
a) Operation of the sled
When the innermost limit switch is ON, the sled moves toward the outer tracks by approx. 1 cm, turning the limit switch ON, then moves toward the inner tracks, again turning the limit switch ON, then stops.
When the innermost limit switch is OFF, the sled moves toward the inner tracks until the limit switch is turned ON.
b) After operation a), the spindle motor starts rotating (approx. 5 sec).

5. Operation of the laser pickup
a) At the same time as the disc motor starts rotating, the laser beam is emitted. If no disc has been loaded, the focus search operation is repeated 9 times.
b) If there is a disc loaded, the first focus search turns the focusing ON, the focusing servo as well as the tracking servo is applied, the lead-in data is read, the number of tracks and total playing time of the disc are displayed, and the player enters standby mode.

6. Play skip and FF (REV) operations
Based on a calculation of the time difference between the present position and the destination position, the destination position is located from the combination of the sled operation and track jump of the tracking operation. The FF (REV) operation is also performed based on the combination of the track jump operation and sled operation.

※1 Laser diode check method
First check that the laser is emitting. (Do not view the laser beam directly.)
Without loading a disc, put the player in play mode and ensure that the pickup lens moves up and down for 30 seconds. Check that the laser beam is emitted during this up and down movement.

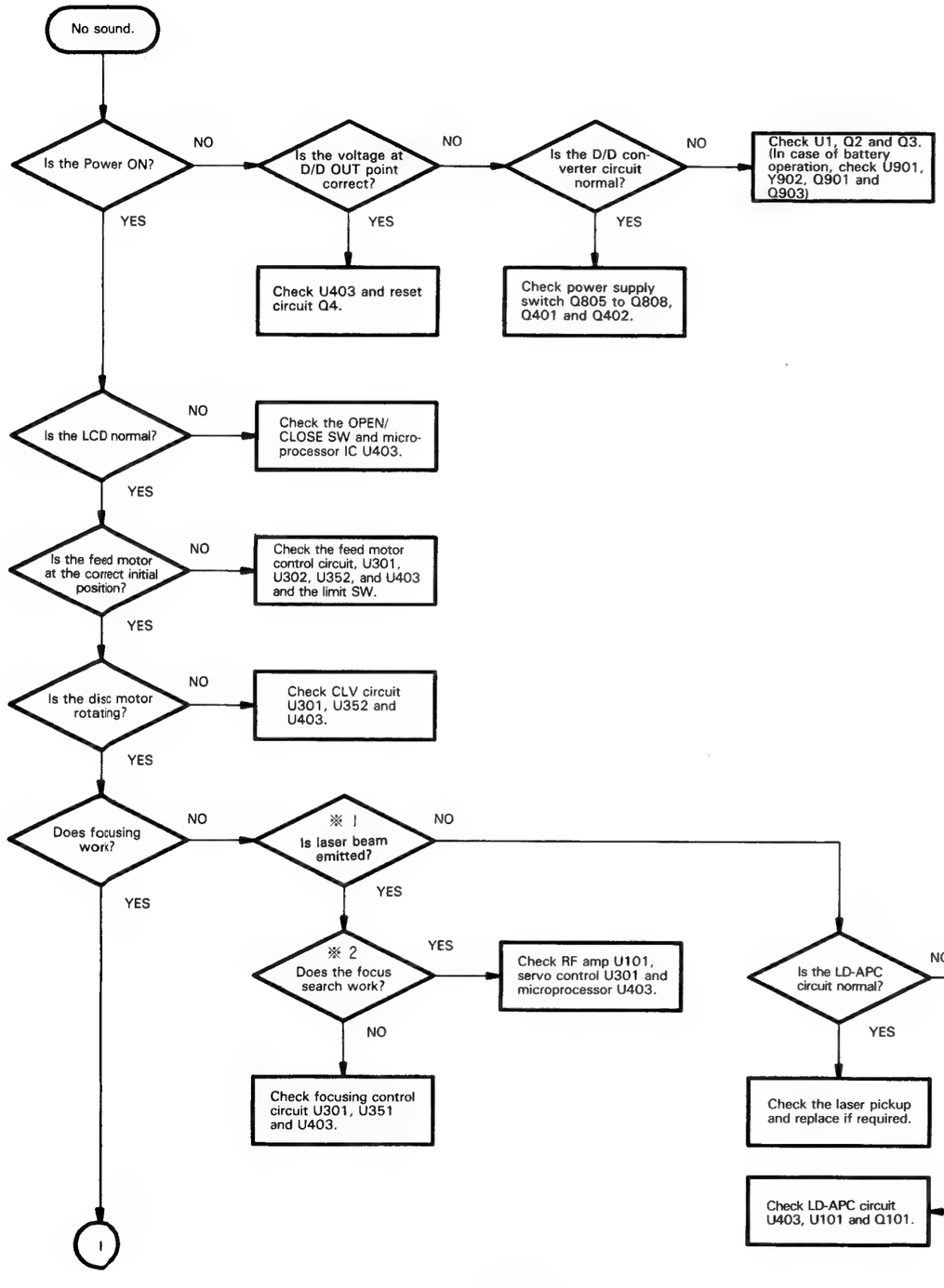
※2 Focus search
With the lid open, switch the OPEN/CLOSE switch forcibly to ON. At this time, the pickup should move from the outer tracks to the inner tracks, and the lens should move up and down. If these do not occur, check the OPEN/CLOSE switch and the limit switch.

※3 Limit switch position
Load a Type 4 test disc (SONY, YEDS-18), and check the position after the TOC has been read.
Connect the TEST pin to GND, display the track time, and set the time display to between 4:00 and 5:20.

※4 Defective disc
If a defective disc cannot be played when the player is operating normally, check the following:
1. Visually check the disc for dirt, pinholes, etc., then play a proper disc and check the RF signal.
2. Check the tracking servo signal waveform to see if the disc is not eccentric.
3. Other
The warp of a disc or the focusing error of a disc can be checked with the focus servo signal.
When the disc is normal, the horizontal and vertical movement should be less than 0.3 mm. If it exceeds this, check the disc table.

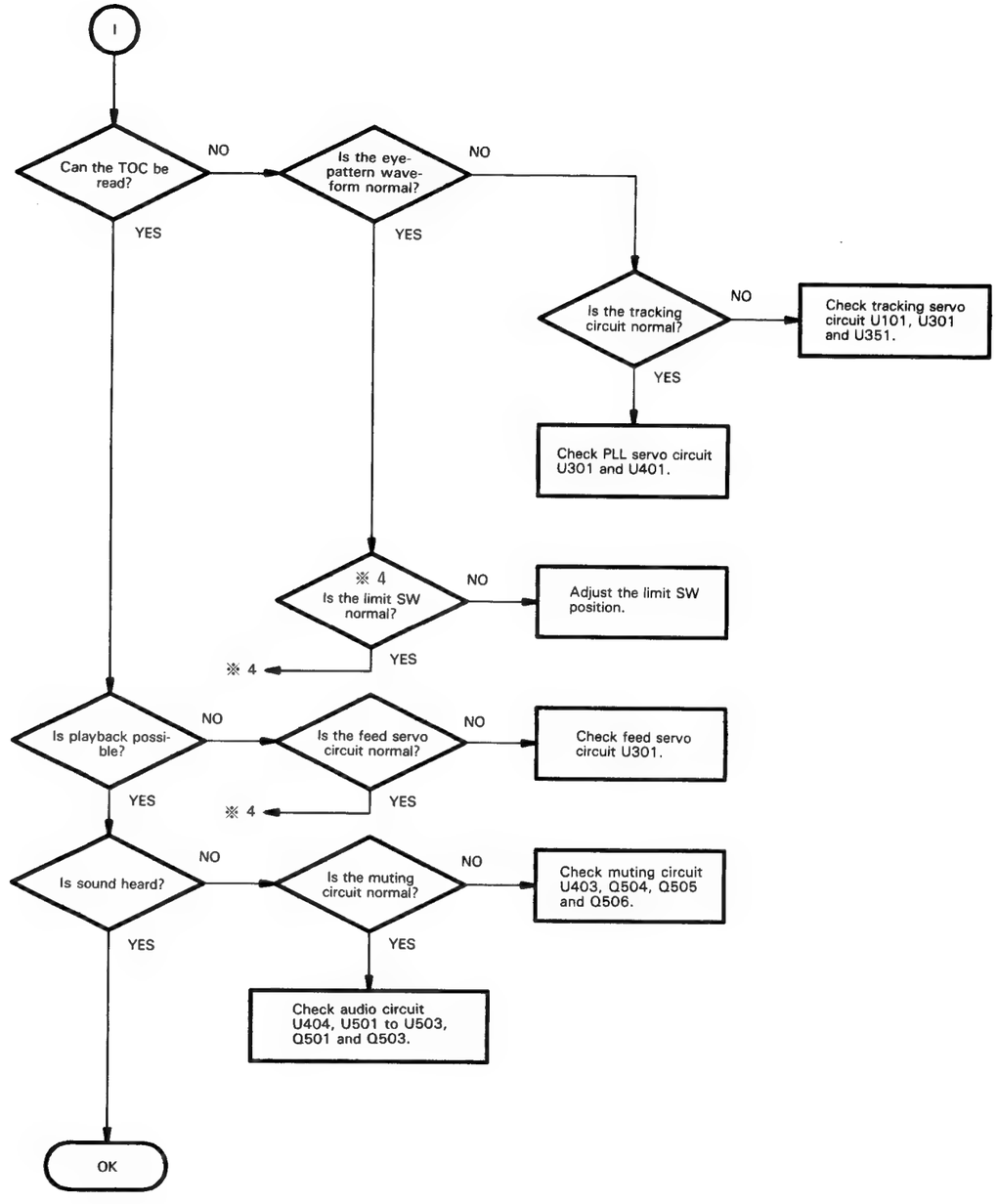
Note: Numbers marked with an ※ correspond to numbers marked with an ※ in "Troubleshooting".

TROUBLESHOOTING



For notes with an asterisk (※) in the above diagram, refer to page 64.

TROUBLESHOOTING



For notes with an asterisk (※) in the above diagram, refer to page 64.

PC BOARD (Component side view)

U351

1	0V
2	2.2V
3	0V
4	4.0V
5	0.6V
6	1.0V
7	1.0V
8	3.5V
9	0V
10	2.4V
11	2.2V
12	0V
13	4.5V
14	4.6V
15	0V
16	4.6V
17	4.5V
18	4.6V
19	0V
20	4.6V
21	4.6V
22	0V

U352

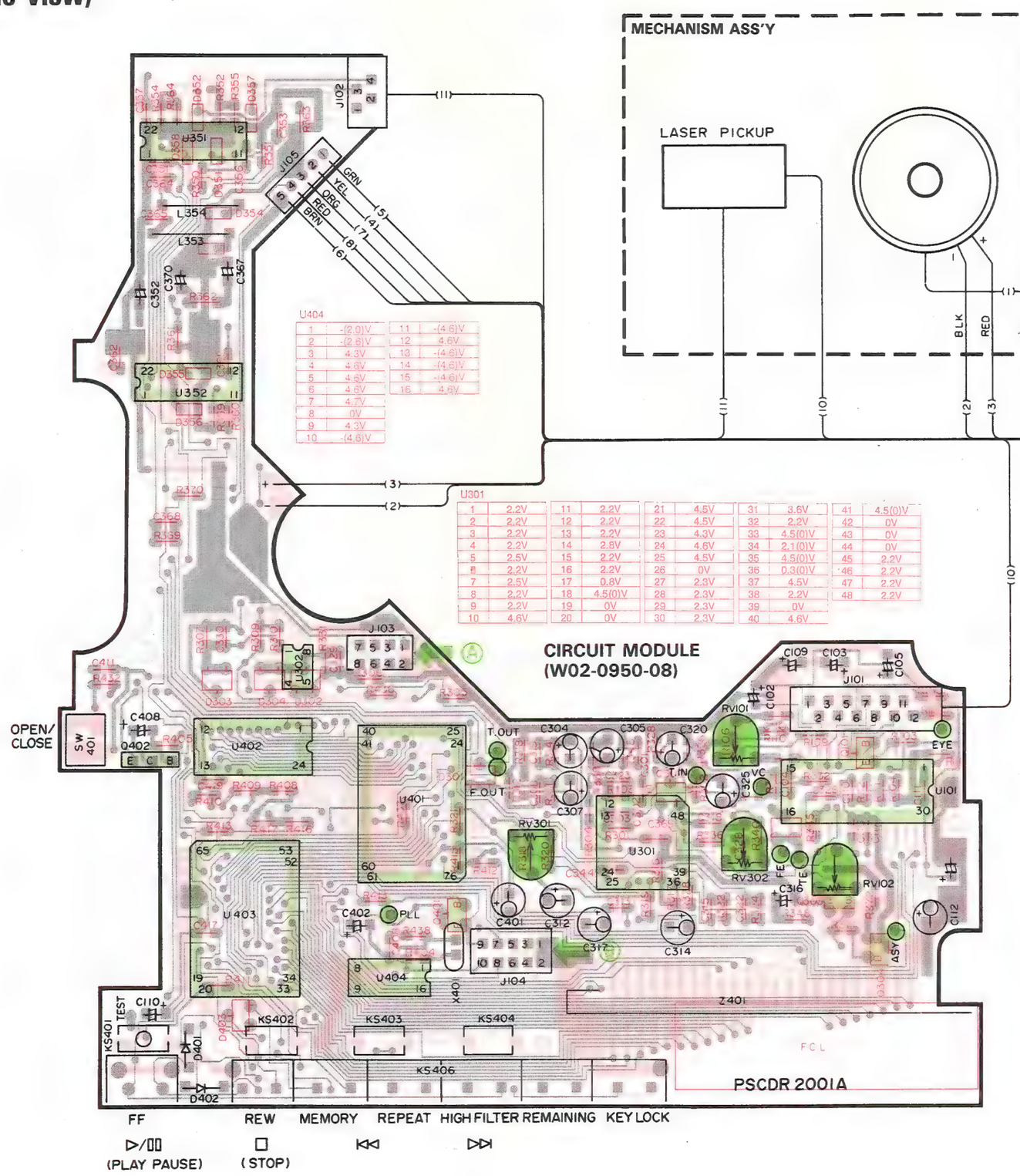
1	0V
2	2.4V
3	0V
4	4.0V
5	1.6V
6	1.0V
7	1.0V
8	3.5V
9	0V
10	2.5(2.3)V
11	2.2V
12	0V
13	4.5V
14	4.6V
15	0V
16	4.6V
17	4.5V
18	4.6V
19	0V
20	4.6V
21	0V
22	0V

U401

1	0.3(0)V	36	-	71	4.6V
2	4.5(0)V	37	-	72	0(4.6)V
3	2.1(0)V	38	-	73	4.6V
4	2.0(0)V	39	-	74	0(4.6)V
5	3.0(2.2)V	40	-	75	4.6V
6	4.6V	41	-	76	4.6V
7	4.5(0)V	42	-	77	4.6V
8	0.75V	43	-	78	4.6(0)V
9	0.65V	44	-	79	4.6V
10	0V	45	-	80	4.6V
11	0V	46	-		
12	0V	47	-		
13	4.5V	48	-		
14	4.6V	49	-		
15	4.3V	50	-		
16	4.5V	51	4.6V		
17	0V	52	0V		
18	4.5(0)V	53	4.6V		
19	0(4.6)V	54	4.3V		
20	3(0)V	55	4.6V		
21	0V	56	0V		
22	0(4.6)V	57	0V		
23	0V	58	0V		
24	4.6(0)V	59	0V		
25	4.5V	60	4.6V		
26	4.5V	61	4.6V		
27	4.6V	62	0V		
28	4.5(0)V	63	0V		
29	-	64	0V		
30	-	65	0V		
31	-	66	0V		
32	-	67	0(4.6)V		
33	4.5V	68	4.6V		
34	-	69	4.6V		
35	-	70	4.6V		

U403

1	0V	26	4.6V	51	-
2	0(4.6)V	27	4.6V	52	-
3	4.6V	28	4.3V	53	-
4	4.5(0)V	29	4.6V	54	-
5	4.6V	30	4.6V	55	3.7V
6	0V	31	-	56	2.3V
7	0V	32	-	57	1.9V
8	4.6(0)V	33	-	58	4.6V
9	0V	34	-	59	0V
10	0(4.6)V	35	-	60	4.0V
11	0V	36	-	61	2.0V
12	4.6V	37	-	62	4.5V
13	4.6V	38	-	63	0V
14	4.6V	39	-	64	0V
15	4.6V	40	-		
16	4.6V	41	-		
17	4.6(0)V	42	-		
18	0(4.5)V	43	-		
19	0.5V	44	-		
20	1.4V	45	-		
21	4.6V	46	-		
22	4.5V	47	-		
23	4.5V	48	-		
24	0V	49	-		
25	0V	50	-		



U404

1	-(2.0)V	11	-(4.6)V
2	-(2.6)V	12	4.6V
3	4.3V	13	-(4.6)V
4	4.6V	14	-(4.6)V
5	4.6V	15	-(4.6)V
6	4.6V	16	4.6V
7	4.7V		
8	0V		
9	4.3V		
10	-(4.6)V		

U301

1	2.2V	11	2.2V	21	4.5V	31	3.6V
2	2.2V	12	2.2V	22	4.5V	32	2.2V
3	2.2V	13	2.2V	23	4.3V	33	4.5(0)V
4	2.2V	14	2.8V	24	4.6V	34	2.1(0)V
5	2.5V	15	2.2V	25	4.5V	35	4.5(0)V
6	2.2V	16	2.2V	26	0V	36	0.3(0)V
7	2.5V	17	0.8V	27	2.3V	37	4.5V
8	2.2V	18	4.5(0)V	28	2.3V	38	2.2V
9	2.2V	19	0V	29	2.3V	39	0V
10	4.6V	20	0V	30	2.3V	40	4.6V

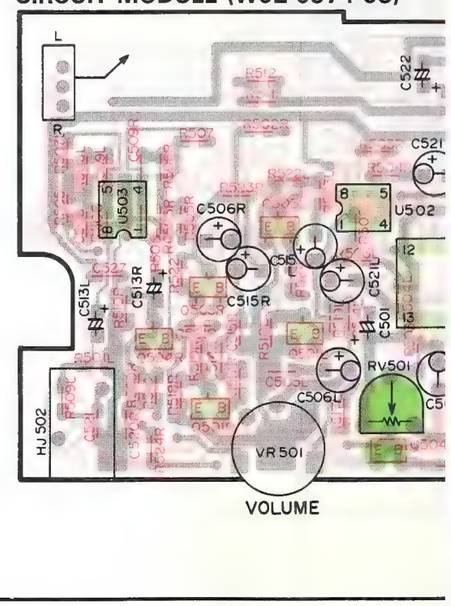
41	4.5(0)V
42	0V
43	0V
44	0V
45	2.2V
46	2.2V
47	2.2V
48	2.2V

U501

1	-
2	-
3	-
4	-
5	1.6V
6	-
7	0V
8	0V
9	0V
10	-(1.7)V
11	2.3V
12	-(1.7)V
13	4.3V
14	4.3V
15	2.2V
16	0V
17	1.4V
18	1.4V
19	4.3V
20	4.3V
21	4.3V
22	-
23	0V
24	4.3V

U101

1	1.0V
2	1.0V
3	2.2V
4	3.2V
5	3.3(0)V
6	0V
7	2.2V
8	2.2V
9	2.2V
10	2.2V
11	2.2V
12	1.4(2.2)V
13	1.7(2.2)V
14	2.2V
15	1.0V
16	1.5(3.2)V
17	0V
18	2.2V
19	2.2V
20	2.2V
21	0V
22	0V
23	2.4(1.8)V
24	2.0V
25	0V
26	2.2V
27	(0)V
28	4.5(0)V
29	1.2(4.5)V
30	4.4V



MECHANISM ASS'Y

LASER PICKUP

YEL (4) GRN (5)

BRN (6)

BLK (1)

LIMIT SW

RED (8)

ORG (7)

BLK

RED

(11) (10) (2) (3) (4,5,6) (7,8)

-(4.6)V
4.6V
-(4.6)V
-(4.6)V
-(4.6)V
4.6V

U301

1	2.2V	11	2.2V	21	4.5V	31	3.6V	41	4.5(0)V
2	2.2V	12	2.2V	22	4.5V	32	2.2V	42	0V
3	2.2V	13	2.2V	23	4.3V	33	4.5(0)V	43	0V
4	2.2V	14	2.8V	24	4.6V	34	2.1(0)V	44	0V
5	2.5V	15	2.2V	25	4.5V	35	4.5(0)V	45	2.2V
6	2.2V	16	2.2V	26	0V	36	0.3(0)V	46	2.2V
7	2.5V	17	0.8V	27	2.3V	37	4.5V	47	2.2V
8	2.2V	18	4.5(0)V	28	2.3V	38	2.2V	48	2.2V
9	2.2V	19	0V	29	2.3V	39	0V		
10	4.6V	20	0V	30	2.3V	40	4.6V		

CIRCUIT MODULE
(W02-0950-08)

C109 C103 C105 C102 U101 RV101 EYE T.OUT C304 C305 C320 F.OUT C307 T.IN C325 VC U101 RV301 U301 RV302 C316 RV102 C401 C312 C317 C314 C112 ASY J104 Z401 KS404 KS406 FCL PSCDR 2001A

U101

1	1.0V
2	1.0V
3	2.2V
4	3.2V
5	3.3(0)V
6	0V
7	2.2V
8	2.2V
9	2.2V
10	2.2V
11	2.2V
12	1.4(2.2)V
13	1.7(2.2)V
14	2.2V
15	1.0V
16	1.5(3.2)V
17	0V
18	2.2V
19	2.2V
20	2.2V
21	0V
22	0V
23	2.4(1.8)V
24	2.0V
25	0V
26	2.2V
27	(0)V
28	4.5(0)V
29	1.2(4.5)V
30	4.4V

AT HIGH FILTER REMAINING KEY LOCK

BLK

RED

BATTERY

U501

1	-
2	-
3	-
4	-
5	1.6V
6	-
7	0V
8	0V
9	0V
10	-(1.7)V
11	2.3V
12	-(1.7)V
13	4.3V
14	4.3V
15	2.2V
16	0V
17	1.4V
18	1.4V
19	4.3V
20	4.3V
21	4.3V
22	-
23	0V
24	4.3V

DC IN LINE OUT DIGITAL OUT

PJ801 D801 HJ501 DJ401

U1

1	3.0V
2	1.8V
3	8.0V
4	0V
5	8.0V
6	1.0V
7	1.3V
8	4.6

C814 L1 D6 C12 C2 T1 P103 C702 C701 SW801 POWER ON◄►OFF Q805 U701 C821 D821 C522 L601 D3 L901 RV1 C809 C801 C3 D802 Q903 D902 D901 U901 C521R U802 U503 C506R C513L C513R C515R C521L C501 U502 U501 C11 P104 D507 D508 C516 D504 Y902 J106 C907 C506L RV501 C503 C502 C511 HJ502 VR501 D506 C902

CIRCUIT MODULE (W02-0974-08)

VOLUME

BLK RED

FRONT

U901

1	1.6V
2	1.0V
3	-
4	0.1V
5	0.9V
6	0V
7	0V
8	-
9	0V
10	-
11	2.7V
12	1.3V
13	1.3V
14	1.4V

Refer to the schematic diagram for the values of resistors and capacitors.

PC BOARD (Foil side view)

U351

1	0V
2	2.2V
3	0V
4	4.0V
5	0.6V
6	1.0V
7	1.0V
8	3.5V
9	0V
10	2.4V
11	2.2V
12	0V
13	4.5V
14	4.6V
15	0V
16	4.6V
17	4.5V
18	4.6V
19	0V
20	4.6V
21	4.6V
22	0V

U352

1	0V
2	2.4V
3	0V
4	4.0V
5	1.6V
6	1.0V
7	1.0V
8	3.5V
9	0V
10	2.5(2.3)V
11	2.2V
12	0V
13	4.5V
14	4.6V
15	0V
16	4.6V
17	4.5V
18	4.6V
19	0V
20	4.6V
21	0V
22	0V

U401

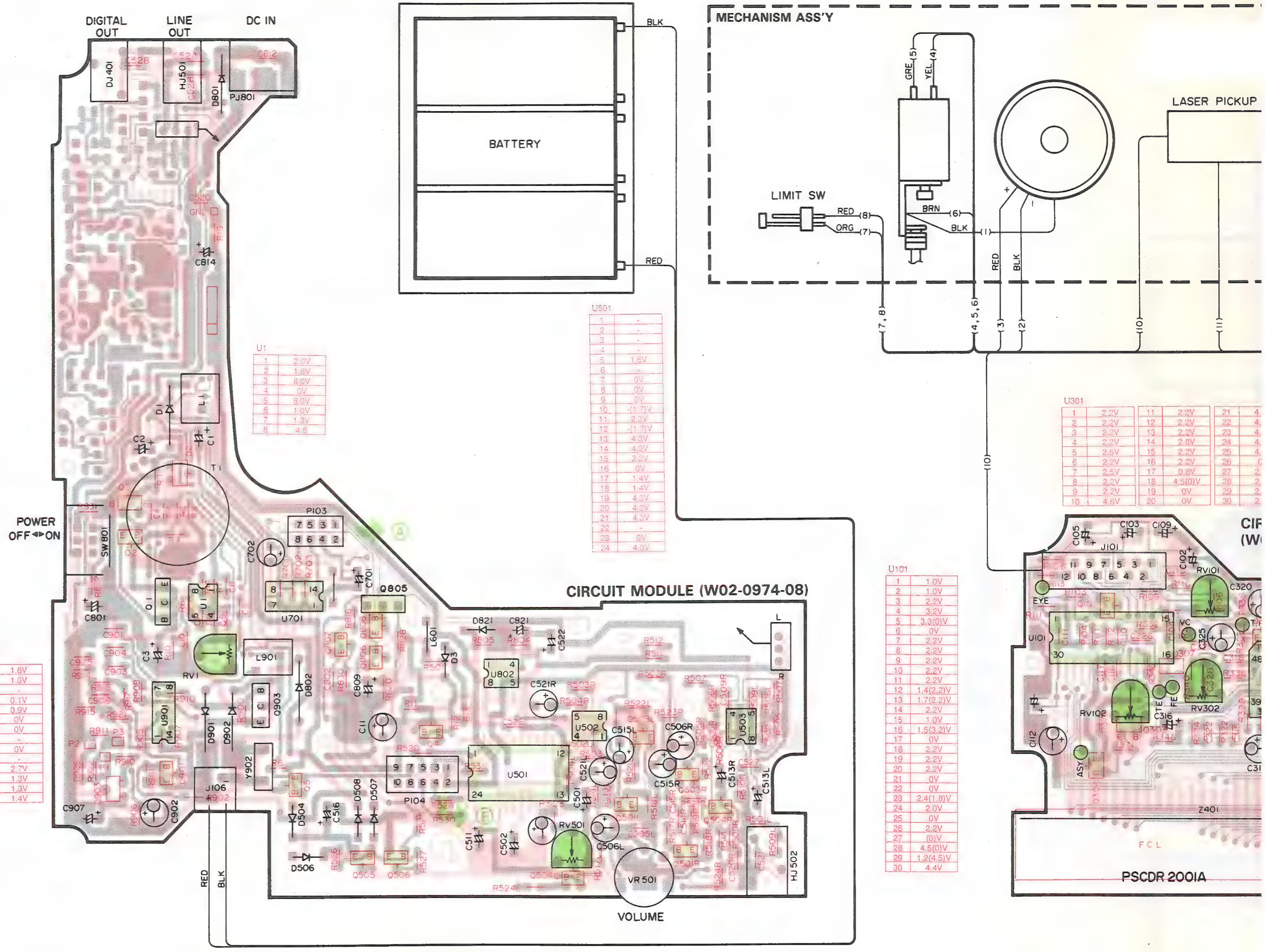
1	0.3(0)V	36	-	71	4.6V
2	4.5(0)V	37	-	72	0(4.6)V
3	2.1(0)V	38	-	73	4.6V
4	2.0(0)V	39	-	74	0(4.6)V
5	3.0(2.2)V	40	-	75	4.6V
6	4.6V	41	-	76	4.6V
7	4.5(0)V	42	-	77	4.6V
8	0.75V	43	-	78	4.6(0)V
9	0.65V	44	-	79	4.6V
10	0V	45	-	80	4.6V
11	0V	46	-		
12	0V	47	-		
13	4.5V	48	-		
14	4.6V	49	-		
15	4.3V	50	-		
16	4.5V	51	4.6V		
17	0V	52	0V		
18	4.5(0)V	53	4.6V		
19	0(4.6)V	54	4.3V		
20	3(0)V	55	4.6V		
21	0V	56	0V		
22	0(4.6)V	57	0V		
23	0V	58	0V		
24	4.6(0)V	59	0V		
25	4.5V	60	4.6V		
26	4.5V	61	4.6V		
27	4.6V	62	0V		
28	4.5(0)V	63	0V		
29	-	64	0V		
30	-	65	0V		
31	-	66	0V		
32	-	67	0(4.6)V		
33	4.5V	68	4.6V		
34	-	69	4.6V		
35	-	70	4.6V		

U403

1	0V	26	4.6V	51	-
2	0(4.6)V	27	4.6V	52	-
3	4.6V	28	4.3V	53	-
4	4.5(0)V	29	4.6V	54	-
5	4.6V	30	4.6V	55	3.7V
6	0V	31	-	56	2.8V
7	0V	32	-	57	1.9V
8	4.6(0)V	33	-	58	4.6V
9	0V	34	-	59	0V
10	0(4.6)V	35	-	60	4.0V
11	0V	36	-	61	2.0V
12	4.6V	37	-	62	4.5V
13	4.6V	38	-	63	0V
14	4.6V	39	-	64	0V
15	4.6V	40	-		
16	4.6V	41	-		
17	4.6(0)V	42	-		
18	0(4.5)V	43	-		
19	0.5V	44	-		
20	1.4V	45	-		
21	4.6V	46	-		
22	4.5V	47	-		
23	4.5V	48	-		
24	0V	49	-		
25	0V	50	-		

U901

1	1.6V
2	1.0V
3	-
4	0.1V
5	0.9V
6	0V
7	0V
8	-
9	0V
10	-
11	2.7V
12	1.3V
13	1.3V
14	1.4V



U1

1	2.0V
2	1.8V
3	8.0V
4	0V
5	8.0V
6	1.0V
7	1.3V
8	4.6

U501

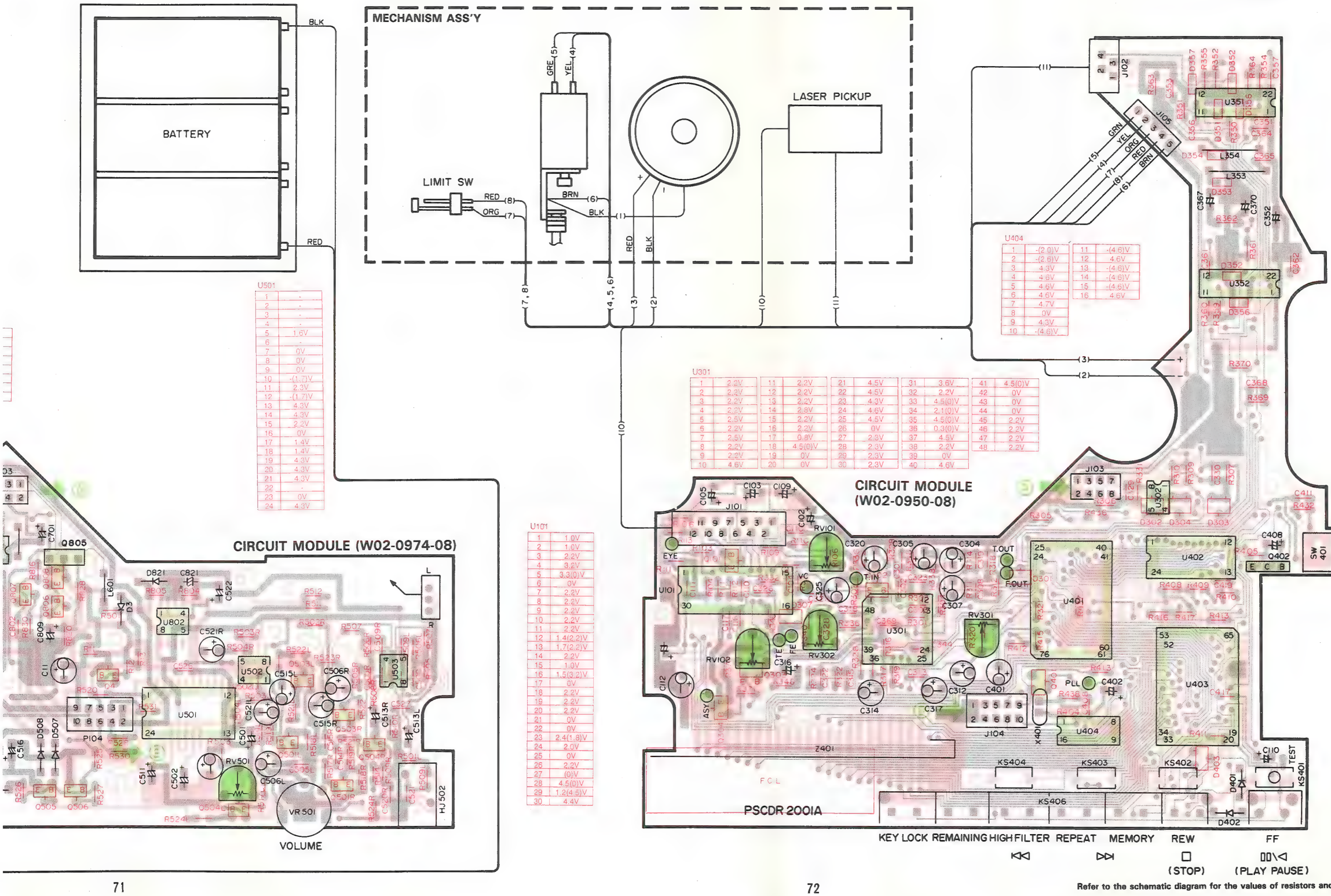
1	-
2	-
3	-
4	-
5	1.6V
6	-
7	0V
8	0V
9	0V
10	-(1.7)V
11	2.3V
12	-(1.7)V
13	4.3V
14	4.3V
15	2.2V
16	0V
17	1.4V
18	1.4V
19	4.3V
20	4.3V
21	4.3V
22	-
23	0V
24	4.3V

U101

1	1.0V
2	1.0V
3	2.2V
4	3.2V
5	3.3(0)V
6	0V
7	2.2V
8	2.2V
9	2.2V
10	2.2V
11	2.2V
12	1.4(2.2)V
13	1.7(2.2)V
14	2.2V
15	1.0V
16	1.5(3.2)V
17	0V
18	2.2V
19	2.2V
20	2.2V
21	0V
22	0V
23	2.4(1.8)V
24	2.0V
25	0V
26	2.2V
27	(0)V
28	4.5(0)V
29	1.2(4.5)V
30	4.4V

U301

1	2.2V	11	2.2V	21	4.
2	2.2V	12	2.2V	22	4.
3	2.2V	13	2.2V	23	4.
4	2.2V	14	2.8V	24	4.
5	2.5V	15	2.2V	25	4.
6	2.2V	16	2.2V	26	0
7	2.5V	17	0.8V	27	2.
8	2.2V	18	4.5(0)V	28	2.
9	2.2V	19	0V	29	2.
10	4.6V	20	0V	30	2.



U501	
1	-
2	-
3	-
4	-
5	1.6V
6	-
7	0V
8	0V
9	0V
10	-(1.7)V
11	2.3V
12	-(1.7)V
13	4.3V
14	4.3V
15	2.2V
16	0V
17	1.4V
18	1.4V
19	4.3V
20	4.3V
21	4.3V
22	-
23	0V
24	4.3V

U404			
1	-(2.6)V	11	-(4.6)V
2	-(2.6)V	12	4.6V
3	4.3V	13	-(4.6)V
4	4.6V	14	-(4.6)V
5	4.6V	15	-(4.6)V
6	4.6V	16	4.6V
7	4.7V		
8	0V		
9	4.3V		
10	-(4.6)V		

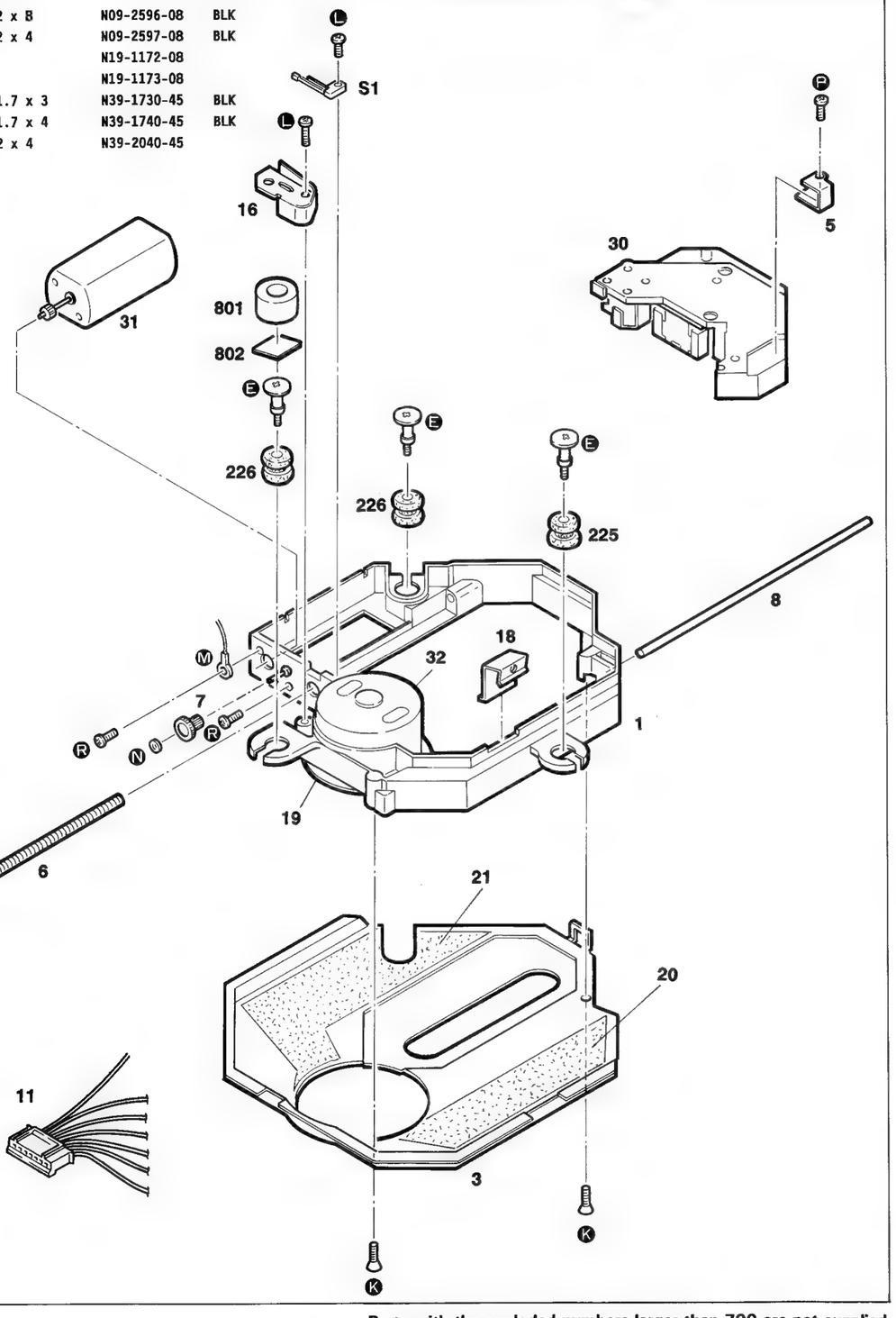
U301							
1	2.2V	11	2.2V	21	4.5V	31	3.6V	41	4.5(0)V
2	2.2V	12	2.2V	22	4.5V	32	2.2V	42	0V
3	2.2V	13	2.2V	23	4.3V	33	4.5(0)V	43	0V
4	2.2V	14	2.8V	24	4.6V	34	2.1(0)V	44	0V
5	2.5V	15	2.2V	25	4.5V	35	4.5(0)V	45	2.2V
6	2.2V	16	2.2V	26	0V	36	0.3(0)V	46	2.2V
7	2.5V	17	0.8V	27	2.3V	37	4.5V	47	2.2V
8	2.2V	18	4.5(0)V	28	2.3V	38	2.2V	48	2.2V
9	2.2V	19	0V	29	2.3V	39	0V		
10	4.6V	20	0V	30	2.3V	40	4.6V		

U101	
1	1.0V
2	1.0V
3	2.2V
4	3.2V
5	3.3(0)V
6	0V
7	2.2V
8	2.2V
9	2.2V
10	2.2V
11	2.2V
12	1.4(2.2)V
13	1.7(2.2)V
14	2.2V
15	1.0V
16	1.5(3.2)V
17	0V
18	2.2V
19	2.2V
20	2.2V
21	0V
22	0V
23	2.4(1.8)V
24	2.0V
25	0V
26	2.2V
27	(0)V
28	4.5(0)V
29	1.2(4.5)V
30	4.4V

Refer to the schematic diagram for the values of resistors and capacitors.

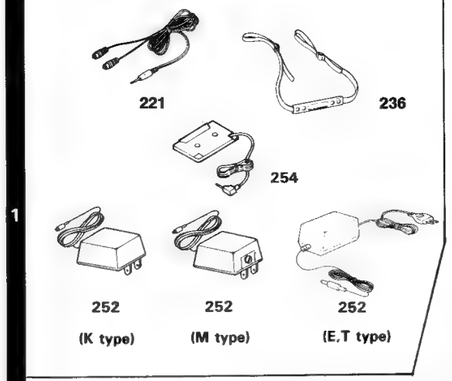
EXPLODED VIEW (MECHANISM)

K	M2 x 8	N09-2596-08	BLK
L	M2 x 4	N09-2597-08	BLK
M		N19-1172-08	
N		N19-1173-08	
P	M1.7 x 3	N39-1730-45	BLK
Q	M1.7 x 4	N39-1740-45	BLK
R	M2 x 4	N39-2040-45	

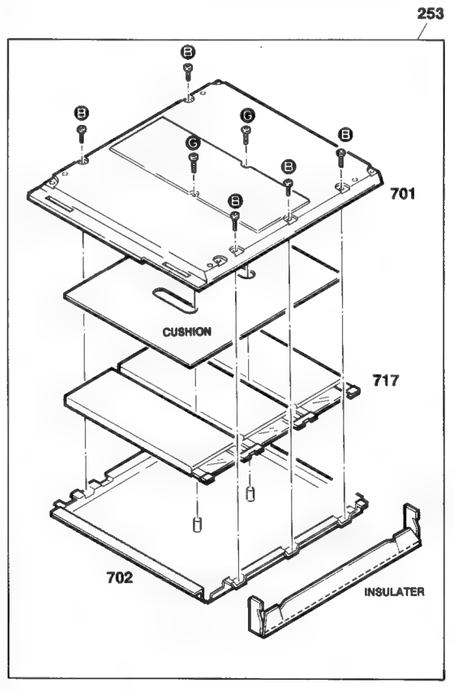


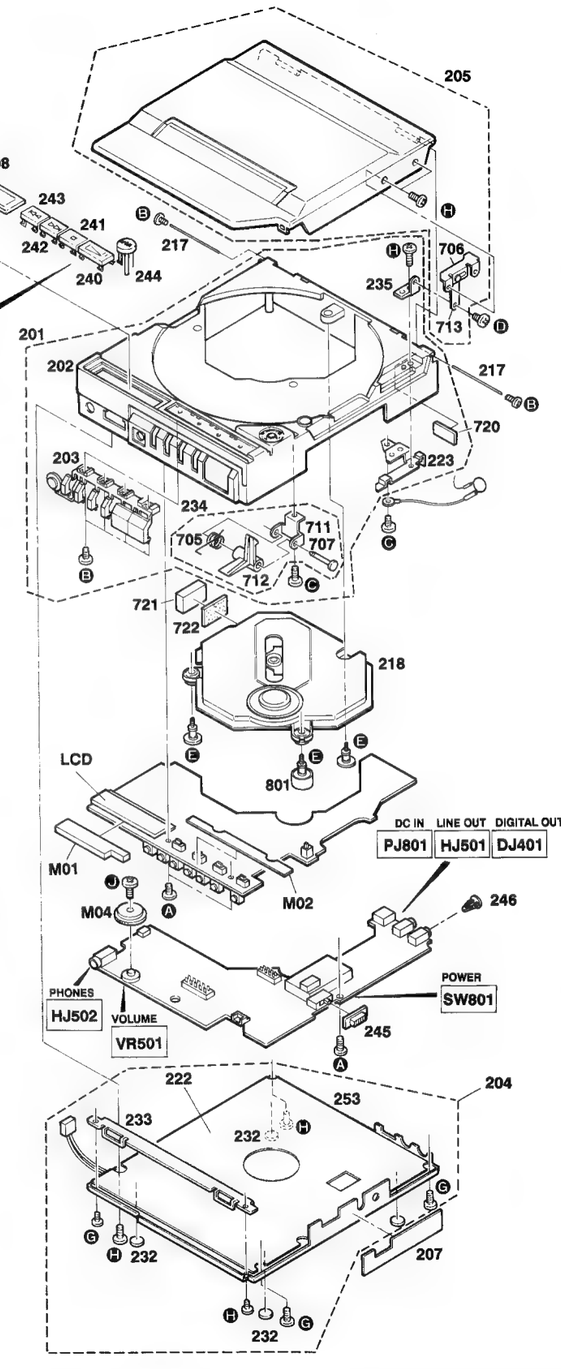
Parts with the exploded numbers larger than 700 are not supplied.

EXPLODED VIEW (UNIT)



R. SKIP	F. SKIP	STOP	PLAY/PAUSE
243	242	241	240





A	M2 x 6	N09-2602-08	BLK
B	M1.7 x 4	N09-2595-08	BLK
C	M2 x 4	N09-2597-08	BLK
D		N09-2598-08	BLK
E		N09-2599-08	
F		N19-1174-08	
G	M1.4 x 3	N39-1430-45	BLK
H	M2 x 2	N39-2020-45	BLK
J	M1.4 x 3	N39-1430-45	BLK

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PARTS LIST

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Ref. No. 参照番号	Address 位置	New Parts 新	Parts No. 部品番号	Description 部品名／規格	Destination 仕向	Remarks 備考
			DPC-77			
201	1D,2D	*	A13-1136-08	FRAME ASSY		
202	1D	*	A13-1137-08	FRAME		
203	2D	*	A13-1138-08	FRAME		
204	3D	*	A40-0965-08	BOTTOM CASE ASSY		
205	1D	*	A52-0125-08	TOP COVER ASSY		
207	3D	*	B07-1868-08	ESCUTCHEON		
208	1C	*	B12-0105-08	DISPLAY WINDOW		
-		*	B46-0177-04	WARRANTY CARD	K	
-		*	B50-9018-08	INSTRUCTION MANUAL		
217	1D	*	D21-1489-08	SHAFT		
218	2D	*	D40-0836-08	MECHANISM ASSY		
221	1C	*	E30-2243-05	AUDIO CORD		
222	3D	*	F20-0998-08	INSULATING SHEET		
223	2D	*	G02-0902-08	LEAF SPRING		
225	2B	*	G11-1304-08	CUSHION (MECHANISM ASSY)		
226	1B,2B	*	G11-1305-08	CUSHION (MECHANISM ASSY)		
-		*	H01-8359-08	ITEM CARTON BOX		
-		*	H11-0020-08	CUSHION		
-		*	H12-2045-18	PACKING FIXTURE		
-		*	H25-0346-08	PROTECTION BAG (INSTRUCTION MANUAL)		
-		*	H25-0347-08	PROTECTION BAG (SHOULDER BELT)		
-		*	H25-0348-08	PROTECTION BAG (UNIT)		
232	3D	*	J02-0392-08	FOOT		
233	3D	*	J19-3070-08	HOLDER		
234	2D	*	J21-5346-08	RETAINER ASSY		
235	1D	*	J21-5347-08	RETAINER		
236	1C	*	J61-0080-08	SHOULDER BELT ASSY		
240	1D	*	K27-1923-08	KNOB(BUTTON) PLAY/PAUSE		
241	1D	*	K27-1933-08	KNOB(BUTTON) STOP		
242	1D	*	K27-1934-08	KNOB(BUTTON) F. SKIP		
243	1D	*	K27-1935-08	KNOB(BUTTON) R. SKIP		
244	1D	*	K27-1936-08	KNOB(BUTTON) OPEN		
245	3D	*	K29-3388-08	KNOB(BUTTON) POWER		
246	2D	*	N29-0260-08	CAP (DIGITAL OUT)		
A	2D,3D	*	N09-2602-08	SCREW (M2 X 6)		
B	1D,2C	*	N09-2595-08	SCREW (M1.7 X 4)		
C	2D		N09-2597-08	SCREW (M2 X 4)		
D	1D	*	N09-2598-08	SCREW		
E	2D	*	N09-2599-08	SCREW		
F		*	N19-1174-08	FLAT WASHER		
G	2C,3D	*	N39-1430-45	SCREW (M1.4 X 3)		
H	1D,3D	*	N39-2020-45	SCREW (M2 X 2)		
⚠ 252	1C	*	W09-0078-08	AC ADAPTOR (120V)	K	
⚠ 252	1C	*	W09-0079-05	AC ADAPTOR (110-120V/220-240V)	M	
⚠ 252	1C	*	W09-0099-08	AC ADAPTOR (220-240V)	E/T	
253	2C	*	W09-0098-08	BATTERY ASSY		
254	1C	*	W01-0153-05	CAR CASSETTE ADAPTOR (CAC-1)		

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PARTS LIST

Ref. No. 参照番号	Address 位置	New Parts 新	Parts No. 部品番号	Description 部品名／規格	Destination 仕向	Remarks 備考
			ELECTRIC UNIT (W02-0950-08)			
C101		*	C90-1691-08	CHIP C 3300pF 50V		
C102		*	C90-1668-08	ELECTRO 100uF 4V		
C103		*	C90-1677-08	ELECTRO 3.3uF 35V		
C104		*	C90-1692-08	CHIP C 0.033uF 50V		
C105		*	C90-1576-08	ELECTRO 33uF 6.3V		
C106		*	C90-1692-08	CHIP C 0.033uF 50V		
C107		*	C90-1684-08	CHIP C 0.01uF 50V		
C108		*	C90-1675-08	ELECTRO 0.47uF 50V		
C109		*	C90-1576-08	ELECTRO 33uF 6.3V		
C110		*	C90-1687-08	CHIP C 1800pF 50V		
C111		*	C90-1690-08	CHIP C 30pF 50V		
C112		*	C90-1678-08	ELECTRO 100uF 6.3V		
C113		*	C90-1686-08	CHIP C 18pF 50V		
C301,C302		*	C90-1681-08	CHIP C 0.047uF 25V		
C303		*	C90-1685-08	CHIP C 150pF 50V		
C304,C305		*	C90-1672-08	ELECTRO 10uF 16V		
C306		*	C90-1669-08	ELECTRO 100uF 6.3V		
C307		*	C90-1675-08	ELECTRO 0.47uF 50V		
C308		*	C90-1688-08	CHIP C 22pF 50V		
C309		*	C90-1689-08	CHIP C 0.022uF 50V		
C312		*	C90-1670-08	ELECTRO 22uF 6.3V		
C313		*	C90-1683-08	CHIP C 1000pF 50V		
C314		*	C90-1675-08	ELECTRO 0.47uF 50V		
C315		*	C90-1692-08	CHIP C 0.033uF 50V		
C316		*	C90-1671-08	ELECTRO 220uF 6.3V		
C317		*	C90-1674-08	ELECTRO 0.33uF 50V		
C318		*	C90-1680-08	CHIP C 0.1uF 25V		
C320		*	C90-1673-08	ELECTRO 0.22uF 50V		
C321		*	C90-1683-08	CHIP C 1000pF 50V		
C322,C323		*	C90-1693-08	CHIP C 39pF 50V		
C325		*	C90-1673-08	ELECTRO 0.22uF 50V		
C326		*	C90-1683-08	CHIP C 1000pF 50V		
C328		*	C90-1693-08	CHIP C 39pF 50V		
C329,C330		*	C90-1689-08	CHIP C 0.022uF 50V		
C334		*	C90-1689-08	CHIP C 0.022uF 50V		
C351		*	C90-1694-08	CHIP C 4700pF 50V		
C352		*	C90-1672-08	ELECTRO 10uF 16V		
C353		*	C90-1696-08	CHIP C 0.22uF 25V		
C356,C357		*	C90-1691-08	CHIP C 3300pF 50V		
C361,C362		*	C90-1684-08	CHIP C 0.01uF 50V		
C364,C365		*	C90-1689-08	CHIP C 0.022uF 50V		
C367		*	C90-1576-08	ELECTRO 33uF 6.3V		
C368,C369		*	C90-1680-08	CHIP C 0.1uF 25V		
C370		*	C90-1678-08	ELECTRO 100uF 6.3V		
C401		*	C90-1676-08	ELECTRO 1uF 50V		
C402		*	C90-1679-08	ELECTRO 33uF 6.3V		
C403,C404		*	C90-1682-08	CHIP C 10pF 50V		
C407		*	C90-1680-08	CHIP C 0.1uF 25V		
C408,C410		*	C90-1672-08	ELECTRO 10uF 16V		
C409		*	C90-1695-08	CHIP C 82pF 50V		
C411		*	C90-1689-08	CHIP C 0.022uF 50V		
D301-D304			MA153	DIODE		

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RV101 EF BALANCE

RV102 F. OFFSET

RV302 TRACKING GAIN

RV301 PLL

LD SWITCH

Q101

U101:CXA1081M RF AMP

U351: BA6280AF PWM DRIVER

U352:BA6280AF PWM DRIVER

U301:CXA1082AQ SERVO CONTROL

U403:CXP5024 MICRO PROCESSOR

U401:CXD1125Q PCM DECODE

U404 SM5807ES

DIGITAL FILTER

U402:LC3517ALM-15 S-RAM

U302 (1/2)

U302 (2/2)

Q401 POWER SW

Q402

U351,U352 POWER SW

FOCUS CONT

T. IN

F. OUT

T. OUT

TRACKING CONT

FOCUS GAIN SW

PLL 4.26MHz

LASER PICKUP

DISC MOTOR

FEED MOTOR

LIMIT SW

SW401 OPEN/CLOSE

(LID)

KS405 FF	KS401 PLAY/PAUSE	
KS406-1 REV	KS402 STOP	
KS403 SKIP ▷▷	KS406-5 REMAINING	
KS404 SKIP ◁◁	KS406-3 REPEAT	

2SA1431
2SA881

2SD601
2SA1036
2SB709
DTC144TK
2SB970
2SD1757K

NJM2352M
NJM3415M
uPC4558G2

LC3517
PCM60P-KY

74HC04
BA9700

CXA1081M

CXA1082AQ

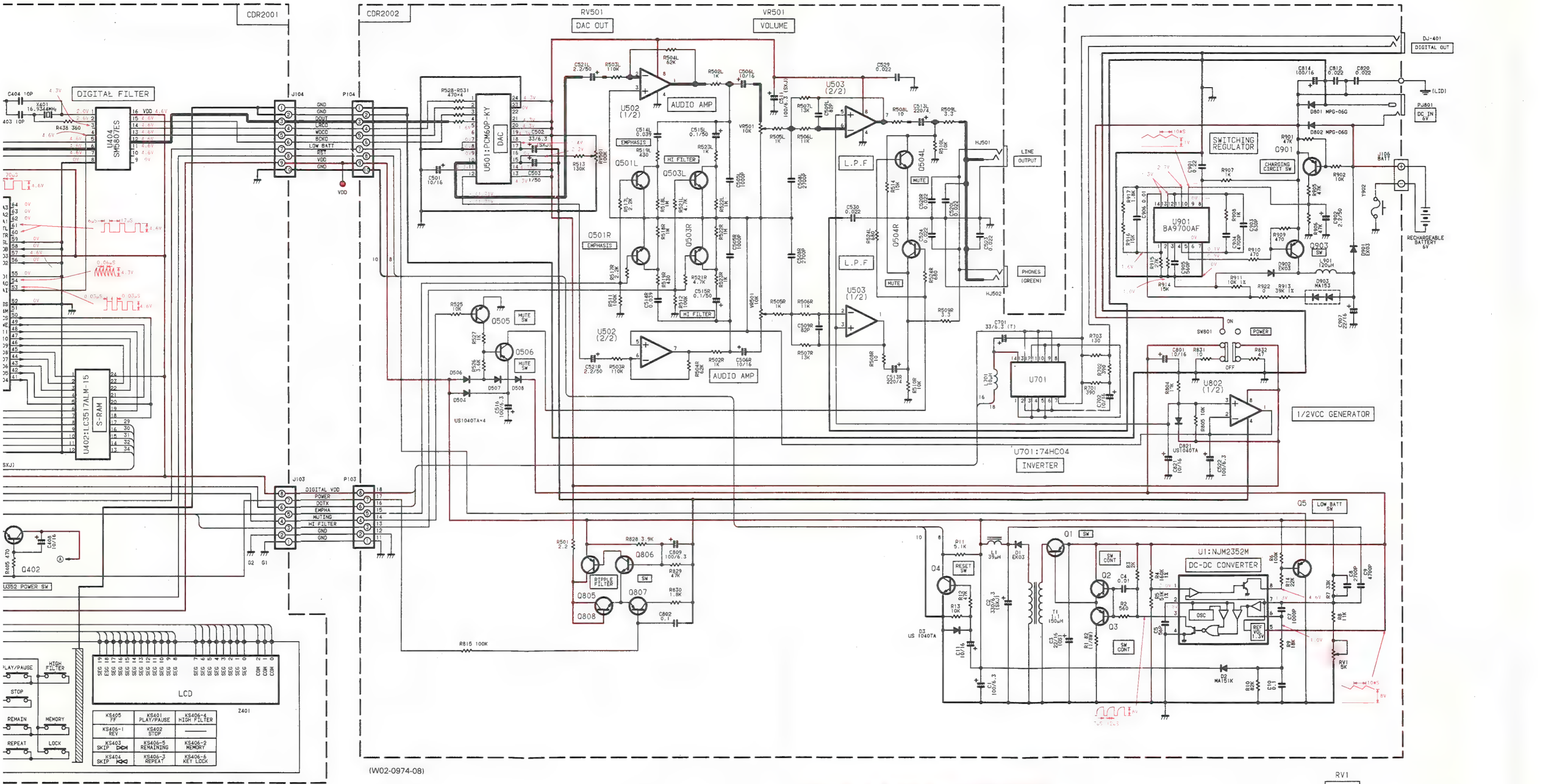
BA6280AF

CXD1125Q

CXP5024H-042Q

SM5807ES

U1
U101
U301
U302,502,503
U351,352
U401
U402
U403
U404
U501
U701
U802
U901



(W02-0950-08)

(W02-0974-08)

U1	NJM2352M	Q1,903	2SA1431(O,Y)	D1	EK-03
U101	CXA1081M	Q2,501,503,505,806,808	2SD601(YR,YS)	D2	MA151K
U301	CXA1082AQ	Q3	2SA1036(HQ,HR)	D3,401-403,504,506-508,821	US1040MTA
U302,502,503	NJM3415M	Q101,304,506,807,901	2SB709(AR,AS)	D301-304,307,903	MA153
U351,352	BA6280AF	Q302,303	DTC144TK	D351-358	RB451F
U401	CXD1125Q	Q401	2SB970	D801,802	MPG06G
U402	LC3517	Q402,805	2SA881(Q,R)	D901,902	EK-03
U403	CXP5024H-042Q	Q504	2SD1757K(AR,AS)	Y902	ICP-F38
U404	SM5807ES				
U501	PCM60P-KY				
U701	74HC04				
U802	uPC4558G2				
U901	BA9700				

DC voltages are as measured with a high impedance voltmeter. Values may vary slightly due to variations between individual instruments or/and units.

Les tensions c.c. doivent être mesurées avec un voltmètre à haute impédance. Les valeurs peuvent différer légèrement du fait des variations inhérentes aux appareils et aux instruments de mesure individuels.

Die angegebenen Gleichspannungswerte wurden mit einem hochohmigen Spannungsmesser gemessen. Dabei schwanken die Meßwerte aufgrund von Unterschieden zwischen einzelnen Instrumenten oder Geräten u.U. geringfügig.

CAUTION: For continued safety, replace safety critical components only with manufacturer's recommended parts (refer to parts list). ⚠ Indicates safety critical components. To reduce the risk of electric shock, leakage-current or resistance measurements shall be carried out (exposed parts are acceptably insulated from the supply circuit) before the appliance is returned to the customer.

SIGNAL LINE
GND LINE
+B LINE

DPC-77

KENWOOD

PARTS LIST

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D307			MA153	DIODE		
D351-D358		*	RB451F	DIODE		
D401-D403		*	US1040MTA	DIODE		
J101		*	E40-3992-08	PIN ASSY		
J102		*	E40-3993-08	PIN ASSY		
J103,J104		*	E40-3995-08	PIN ASSY		
J105		*	E40-3994-08	PIN ASSY		
KS401		*	S40-1131-08	PUSH SWITCH (PLAY/PAUSE)		
KS402		*	S40-1131-08	PUSH SWITCH (STOP)		
KS403		*	S40-1131-08	PUSH SWITCH (F. SKIP)		
KS404		*	S40-1131-08	PUSH SWITCH (R. SKIP)		
KS405		*	S40-1132-08	PUSH SWITCH (FF)		
KS406		*	S40-1133-08	PUSH SWITCH (REV, MEMORY REPEAT HIGH FILTTER KEY LOCK)		
L353,L354		*	L33-0349-08	CHOKE COIL		
M01		*	J39-0146-08	SPACER		
M02		*	G16-0705-08	SHEET		
Q101		*	2SB709(AR,AS)	TRANSISTOR		
Q302,Q303			DTC144TK	TRANSISTOR		
Q304		*	2SB709(AR,AS)	TRANSISTOR		
Q401		*	2SB970	TRANSISTOR		
Q402		*	2SA881(Q,R)	TRANSISTOR		
R101			RK73FB1J222J	CHIP R 2.2K J 1/16W		
R103			RK73FB1J100J	CHIP R 10 J 1/16W		
R104			RK73FB1J822J	CHIP R 8.2K J 1/16W		
R105			RK73FB1J223J	CHIP R 22K J 1/16W		
R106			RK73FB1J102J	CHIP R 1.0K J 1/16W		
R109			RK73EB2A102J	CHIP R 1.0K J 1/10W		
R110			RK73FB1J563J	CHIP R 56K J 1/16W		
R111			RK73FB1J163J	CHIP R 16K J 1/16W		
R112			RK73FB1J103J	CHIP R 10K J 1/16W		
R113			RK73FB1J910J	CHIP R 91 J 1/16W		
R301			RK73FB1J104J	CHIP R 100K J 1/16W		
R302			RK73FB1J432J	CHIP R 4.3K J 1/16W		
R303			RK73FB1J334J	CHIP R 330K J 1/16W		
R304			RK73FB1J563J	CHIP R 56K J 1/16W		
R305			RK73FB1J103J	CHIP R 10K J 1/16W		
R306			RK73FB1J432J	CHIP R 4.3K J 1/16W		
R307			RK73FB1J183J	CHIP R 18K J 1/16W		
R308,R309			RK73FB1J222J	CHIP R 2.2K J 1/16W		
R310			RK73FB1J432J	CHIP R 4.3K J 1/16W		
R311			RK73FB1J104J	CHIP R 100K J 1/16W		
R312			RK73FB1J472J	CHIP R 4.7K J 1/16W		
R314			RK73FB1J684J	CHIP R 680K J 1/16W		
R316,R317			RK73FB1J104J	CHIP R 100K J 1/16W		
R318			RK73FB1J103J	CHIP R 10K J 1/16W		
R319			RK73FB1J913J	CHIP R 91K J 1/16W		
R320			RK73FB1J362J	CHIP R 3.6K J 1/16W		
R321			RK73FB1J104J	CHIP R 100K J 1/16W		
R322			RK73FB1J105J	CHIP R 1.0M J 1/16W		
R323			RK73FB1J203J	CHIP R 20K J 1/16W		

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R324,R328			RK73FB1J334J	CHIP R 330K J 1/16W		
R331			RK73FB1J183J	CHIP R 18K J 1/16W		
R332			RK73FB1J103J	CHIP R 10K J 1/16W		
R335			RK73FB1J123J	CHIP R 12K J 1/16W		
R336			RK73FB1J822J	CHIP R 8.2K J 1/16W		
R338			RK73FB1J824J	CHIP R 820K J 1/16W		
R340			RK73FB1J333J	CHIP R 33K J 1/16W		
R343			RK73FB1J473J	CHIP R 47K J 1/16W		
R345			RK73FB1J103J	CHIP R 10K J 1/16W		
R347			RK73FB1J274J	CHIP R 270K J 1/16W		
R348			RK73FB1J100J	CHIP R 10 J 1/16W		
R350			RK73FB1J152J	CHIP R 1.5K J 1/16W		
R351			RK73FB1J472J	CHIP R 4.7K J 1/16W		
R352			RK73EB2A102J	CHIP R 1.0K J 1/10W		
R354			RK73FB1J2R2J	CHIP R 2.2 J 1/16W		
R355			RK73EB2A102J	CHIP R 1.0K J 1/10W		
R359,R360			RK73FB1J2R2J	CHIP R 2.2 J 1/16W		
R361			RK73EB2A102J	CHIP R 1.0K J 1/10W		
R362,R363			RK73EB2A102J	CHIP R 1.0K J 1/10W		
R369			RK73FB1J183J	CHIP R 18K J 1/16W		
R370			RK73FB1J152J	CHIP R 1.5K J 1/16W		
R371			RK73FB1J473J	CHIP R 47K J 1/16W		
R372			RK73FB1J163J	CHIP R 16K J 1/16W		
R402			RK73FB1J103J	CHIP R 10K J 1/16W		
R403			RK73FB1J102J	CHIP R 1.0K J 1/16W		
R405			RK73FB1J471J	CHIP R 470 J 1/16W		
R406-R408			RK73FB1J473J	CHIP R 47K J 1/16W		
R409			RK73FB1J104J	CHIP R 100K J 1/16W		
R410			RK73FB1J681J	CHIP R 680 J 1/16W		
R411			RK73FB1J103J	CHIP R 10K J 1/16W		
R413			RK73FB1J303J	CHIP R 30K J 1/16W		
R415			RK73FB1J134J	CHIP R 130K J 1/16W		
R416-R419			RK73FB1J471J	CHIP R 470 J 1/16W		
R432			RK73FB1J102J	CHIP R 1.0K J 1/16W		
R436			RK73FB1J471J	CHIP R 470 J 1/16W		
R437			RK73FB1J473J	CHIP R 47K J 1/16W		
RV101			R12-3161-08	TRIMMING POT.(20K) EF BALANCE		
RV102			R12-4036-08	TRIMMING POT.(50K) F. OFFSET		
RV301			R12-1110-08	TRIMMING POT. (2K) VCOF		
RV302			R12-3161-08	TRIMMING POT.(20K) TRACKING GAIN		
SW401		*	S50-1049-08	MICRO SWITCH (OPEN/CLOSE)		
U101			CXA1081M	IC (RF AMP)		
U301			CXA1082AQ	IC (SERVO AMP)		
U302			NJM3415M	IC (OP AMP)		
U351,U352		*	BA6280AF	IC (PWM DRIVER)		
U401			CXD1125Q	IC (PCM DECODER)		
U402		*	LC3517ALM-15	IC (S-RAM)		
U403		*	CXP5024H-042Q	IC (MICRO PROCESSOR)		
U404		*	SM5807ES	IC (DIGITAL FILTER)		
X401		*	L77-1142-08	CRYSTAL OSC (16.93440 MHz)		
ZL401		*	B38-0115-08	LCD		

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ELECTRIC UNIT (W02-0974-08)						
J			N39-1430-45	SCREW (M1.4 X 3)		
C1		*	C90-1669-08	ELECTRO 100uF 6.3V		
C2		*	C90-1697-08	ELECTRO 330uF 6.3V		
C3		*	C90-1698-08	ELECTRO 22uF 16V		
C4		*	C90-1712-08	CHIP C 0.01uF 50V		
C5		*	C90-1720-08	CHIP C 56pF 50V		
C7		*	C90-1711-08	CHIP C 1000pF 50V		
C8		*	C90-1716-08	CHIP C 2700pF 50V		
C9		*	C90-1719-08	CHIP C 4700pF 50V		
C10		*	C90-1706-08	CHIP C 0.1uF 25V		
C11		*	C90-1672-08	ELECTRO 10uF 16V		
C501		*	C90-1672-08	ELECTRO 10uF 16V		
C502		*	C90-1679-08	ELECTRO 33uF 6.3V		
C503		*	C90-1704-08	ELECTRO 1uF 50V		
C505		*	C90-1711-08	CHIP C 1000pF 50V		
C506		*	C90-1672-08	ELECTRO 10uF 16V		
C508		*	C90-1716-08	CHIP C 2700pF 50V		
C509		*	C90-1695-08	CHIP C 82pF 50V		
C511		*	C90-1678-08	ELECTRO 100uF 6.3V		
C513		*	C90-1699-08	ELECTRO 220uF 4V		
C514		*	C90-1718-08	CHIP C 0.039uF 50V		
C515		*	C90-1703-08	ELECTRO 0.1uF 50V		
C516		*	C90-1669-08	ELECTRO 100uF 6.3V		
C520		*	C90-1689-08	CHIP C 0.022uF 50V		
C521		*	C90-1705-08	ELECTRO 2.2uF 50V		
C522		*	C90-1669-08	ELECTRO 100uF 6.3V		
C523,524		*	C90-1689-08	CHIP C 0.022uF 50V		
C701		*	C90-1576-08	ELECTRO 33uF 6.3V		
C702,801		*	C90-1672-08	ELECTRO 10uF 16V		
C802		*	C90-1725-08	CHIP C 0.1uF 50V		
C809		*	C90-1669-08	ELECTRO 100uF 6.3V		
C812		*	C90-1689-08	CHIP C 0.022uF 50V		
C814		*	C90-1701-08	ELECTRO 100uF 16V		
C821		*	C90-1672-08	ELECTRO 10uF 16V		
C902		*	C90-1705-08	ELECTRO 2.2uF 50V		
C903		*	C90-1723-08	CHIP C 680pF 50V		
C904		*	C90-1719-08	CHIP C 4700pF 50V		
C905		*	C90-1722-08	CHIP C 560pF 50V		
C906		*	C90-1712-08	CHIP C 0.01uF 50V		
C907		*	C90-1702-08	ELECTRO 22uF 16V		
D1		*	EK-03	DIODE		
D2			MA151K	DIODE		
D3			US1040MTA	DIODE		
D504,D506			US1040MTA	DIODE		
D507,D508			US1040MTA	DIODE		
D801,D802		*	MPG06G	DIODE		
D821			US1040MTA	DIODE		
D901,D902		*	EK-03	DIODE		
D903			MA153	DIODE		

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DJ401		*	E11-0187-08	PHONE JACK (DIGITAL OUT)		
FL601		*	L79-0768-08	LC FILTER		
HJ501		*	E11-0185-08	PHONE JACK (LINE OUT)		
HJ502		*	E11-0186-08	PHONE JACK (PHONES)		
L1		*	L33-0351-08	CHOKE COIL		
L701		*	L33-0352-08	CHOKE COIL		
L901		*	L33-0350-08	CHOKE COIL		
M04		*	K29-3387-08	KNOB (VOLUME)		
M07		*	E23-0326-08	TERMINAL		
P101		*	E31-4654-08	WIRE CONNECTOR		
P103,P104		*	E23-0325-08	TERMINAL		
PJ801		*	E03-0098-08	DC JACK (DC IN)		
Q1		*	2SA1431(O,Y)	TRANSISTOR		
Q2		*	2SD601(YR,YS)	TRANSISTOR		
Q3		*	2SA1036(HQ,HR)	TRANSISTOR		
Q501,Q503		*	2SD601(YR,YS)	TRANSISTOR		
Q504		*	2SD1757K(AR,AS)	TRANSISTOR		
Q505		*	2SD601(YR,YS)	TRANSISTOR		
Q506		*	2SB709(AR,AS)	TRANSISTOR		
Q805		*	2SA881(Q,R)	TRANSISTOR		
Q806		*	2SD601(YR,YS)	TRANSISTOR		
Q807		*	2SB709(AR,AS)	TRANSISTOR		
Q808		*	2SD601(YR,YS)	TRANSISTOR		
Q901		*	2SB709(AR,AS)	TRANSISTOR		
Q903		*	2SA1431(O,Y)	TRANSISTOR		
R1			RK73EB2B820J	CHIP R 82 J 1/8W		
R2			RK73FB1J561J	CHIP R 560 J 1/16W		
R3			RK73FB1J202J	CHIP R 2K J 1/16W		
R4			RK73FB1J1603F	CHIP R 160K F 1/16W		
R5			RK73FB1J5102F	CHIP R 51K F 1/16W		
R6			RK73FB1J104J	CHIP R 100K J 1/16W		
R7			RK73FB1J333J	CHIP R 33K J 1/16W		
R8			RK73FB1J912J	CHIP R 9.1K J 1/16W		
R9			RK73FB1J183J	CHIP R 18K J 1/16W		
R10			RK73FB1J823J	CHIP R 82K J 1/16W		
R11			RK73FB1J512J	CHIP R 5.1K J 1/16W		
R501			RK73FB1J2R2J	CHIP R 2.2 J 1/16W		
R502			RK73FB1J102J	CHIP R 1K J 1/16W		
R503			RK73FB1J114J	CHIP R 110K J 1/16W		
R504			RK73FB1J623J	CHIP R 62K J 1/16W		
R505			RK73FB1J102J	CHIP R 1K J 1/16W		
R506			RK73FB1J113J	CHIP R 11K J 1/16W		
R507			RK73FB1J133J	CHIP R 13K J 1/16W		
R508			RK73FB1J100J	CHIP R 10 J 1/16W		
R509			RK73FB1J3R3J	CHIP R 3.3 J 1/16W		
R510			RK73FB1J103J	CHIP R 10K J 1/16W		
R511,R512			RK73FB1J104J	CHIP R 100K J 1/16W		
R513			RK73FB1J134J	CHIP R 130K J 1/16W		

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R514			RK73FB1J153J	CHIP R 15K J 1/16W		
R517			RK73FB1J222J	CHIP R 2.2K J 1/16W		
R518			RK73FB1J105J	CHIP R 1M J 1/16W		
R519			RK73FB1J431J	CHIP R 430 J 1/16W		
R521			RK73FB1J472J	CHIP R 4.7K J 1/16W		
R522			RK73FB1J105J	CHIP R 1M J 1/16W		
R523			RK73FB1J102J	CHIP R 1K J 1/16W		
R524			RK73FB1J681J	CHIP R 680 J 1/16W		
R525			RK73FB1J103J	CHIP R 10K J 1/16W		
R526			RK73FB1J362J	CHIP R 3.6K J 1/16W		
R527			RK73FB1J102J	CHIP R 1K J 1/16W		
R601			RK73FB1J273J	CHIP R 27K J 1/16W		
R602			RK73FB1J912J	CHIP R 9.1K J 1/16W		
R603			RK73FB1J333J	CHIP R 33K J 1/16W		
R604			RK73FB1J822J	CHIP R 8.2K J 1/16W		
R605			RK73FB1J332J	CHIP R 3.3K J 1/16W		
R606			RK73FB1J134J	CHIP R 130K J 1/16W		
R607			RK73FB1J103J	CHIP R 10K J 1/16W		
R608			RK73FB1J202J	CHIP R 2K J 1/16W		
R609			RK73FB1J100J	CHIP R 10 J 1/16W		
R610,611			RK73FB1J101J	CHIP R 100 J 1/16W		
R612			RK73FB1J152J	CHIP R 1.5K J 1/16W		
R613			RK73FB1J753J	CHIP R 75K J 1/16W		
R614			RK73FB1J104J	CHIP R 100K J 1/16W		
R615			RK73FB1J271J	CHIP R 270 J 1/16W		
R616			RK73FB1J272J	CHIP R 2.7K J 1/16W		
R701,702			RK73FB1J391J	CHIP R 390 J 1/16W		
R804,805			RK73FB1J103J	CHIP R 10K J 1/16W		
R815			RK73FB1J104J	CHIP R 100K J 1/16W		
R828			RK73FB1J392J	CHIP R 3.9K J 1/16W		
R829			RK73FB1J473J	CHIP R 47K J 1/16W		
R830			RK73FB1J182J	CHIP R 1.8K J 1/16W		
R831			RK73FB1J100J	CHIP R 10 J 1/16W		
R832			RK73FB1J470J	CHIP R 47 J 1/16W		
R901			RK73FB1J473J	CHIP R 47K J 1/16W		
R902			RK73FB1J103J	CHIP R 10K J 1/16W		
R905,906			RK73FB1J473J	CHIP R 47K J 1/16W		
R907,908			RK73FB1J102J	CHIP R 1K J 1/16W		
R909,R910			RK73FB1J471J	CHIP R 470 J 1/16W		
R911			RK73FB1J1002F	CHIP R 10K F 1/16W		
R913			RK73FB1J3902F	CHIP R 39K F 1/16W		
R914			RK73FB1J153J	CHIP R 15K J 1/16W		
R915			RK73FB1J273J	CHIP R 27K J 1/16W		
R916			RK73FB1J153J	CHIP R 15K J 1/16W		
R917			RK73FB1J182J	CHIP R 1.8K J 1/16W		
R921			RK73FB1J244J	CHIP R 240K J 1/16W		
R922,923			RK73FB1J681J	CHIP R 680 J 1/16W		
RV1		*	R12-2047-08	TRIMMING POT.(5K) VDD		
RV501		*	R12-5076-08	TRIMMING POT.(100K) DAC OUT		
SW801		*	S31-2142-08	SLIDE SWITCH POWER		
T1		*	L19-0060-08	CONVERTER TRANSFORMER		

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U1			NJM2352M	IC (DC-DC CONVERTER)		
U501		*	PCM60P-KY	IC (D/A CONVERTER)		
U502			NJM3415M	IC (AUDIO AMP)		
U503			NJM3415M	IC (L.P.F)		
U701		*	74HC04	IC (DIGITAL OUT)		
U802		*	uPC4558G2	IC (1/2VCC)		
U901		*	BA9700AF	IC (CHARGER CIRCUIT)		
VR501		*	R10-3037-08	POTENTIOMETER(10K) (VOLUME)		
Y902			ICP-F38	IC PROTECTOR		
MECHANISM ASS'Y (D40-0836-08)						
1	2B	*	A10-1846-08	SUB CHASSIS		
3	3B	*	B07-1846-08	ESCUTCHEON		
5	1B	*	D10-2242-08	ARM ASSY		
6	2A	*	D13-0734-08	GEAR ASSY		
7	2A	*	D13-0735-08	GEAR		
8	2B	*	D21-1488-08	SHAFT		
11	3A	*	E31-4656-08	LEAD WIRE		
16	1A	*	G02-0498-08	LEAF SPRING ASSY		
18	2B	*	J11-0133-08	CLAMPER		
19	2A	*	J19-3065-08	HOLDER		
20	3B	*	J69-0064-08	D.F ADHESIVE SHEET		
21	3A	*	J69-0065-08	D.F ADHESIVE SHEET		
K	3B	*	N09-2596-08	SCREW (M2 X 8)		
L	1A	*	N09-2597-08	SCREW (M2 X 4)		
M	2A	*	N19-1172-08	SPRING WASHER		
N	2A	*	N19-1173-08	FLAT WASHER		
P	1B	*	N39-1730-45	SCREW (M1.7 X 3)		
Q	2A	*	N39-1740-45	SCREW (M1.7 X 4) DC MOTOR		
R	2A	*	N39-2040-45	SCREW (M2 X 4)		
S1	1A	*	S46-1119-08	LEAF SWITCH (LIMIT)		
30	1B	*	T31-0050-08	PICKUP ASSY (LASER PICKUP)		
31	1A	*	T42-0488-08	MOTOR ASSY		
32	2A	*	T42-0489-08	DC MOTOR		

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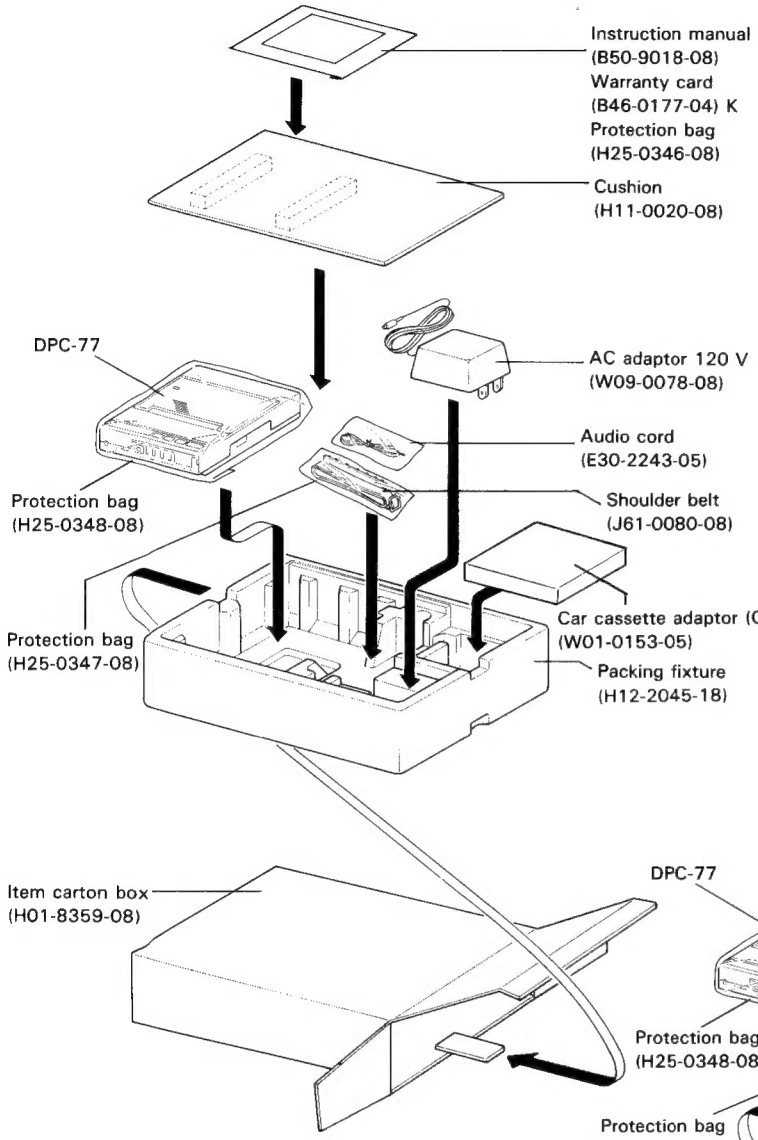
PACKING

(K type only)



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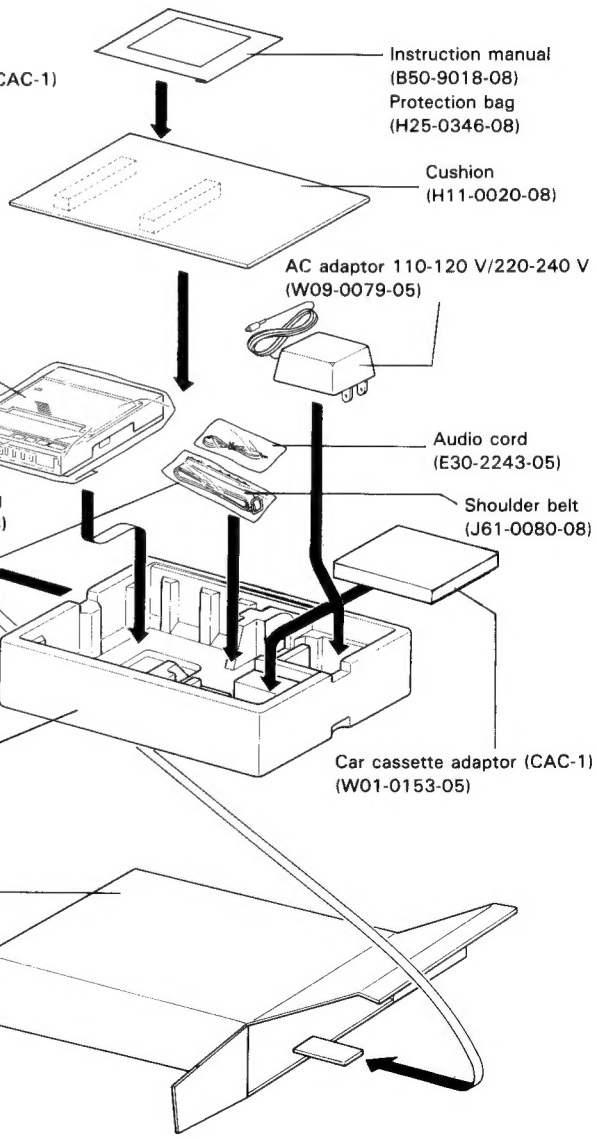

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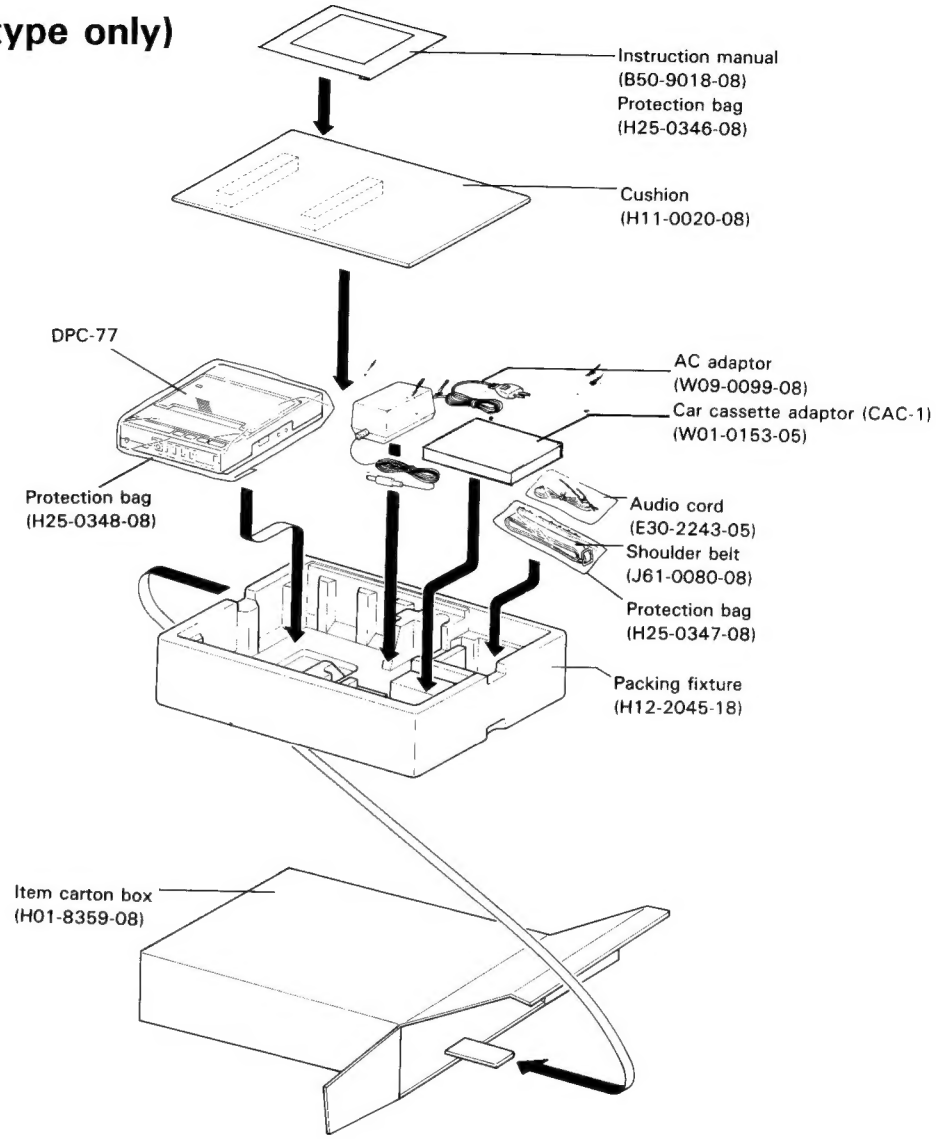
PACKING

(E, T type only)



Note:

Component and circuitry are subject to modification to insure best operation under differing local conditions. This manual is based on, the U.S. (K) standard, and provides information on regional circuit modification through use of alternate schematic diagrams, and information on regional component variations through use of parts list.

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